

FIG. 1
PRIOR ART

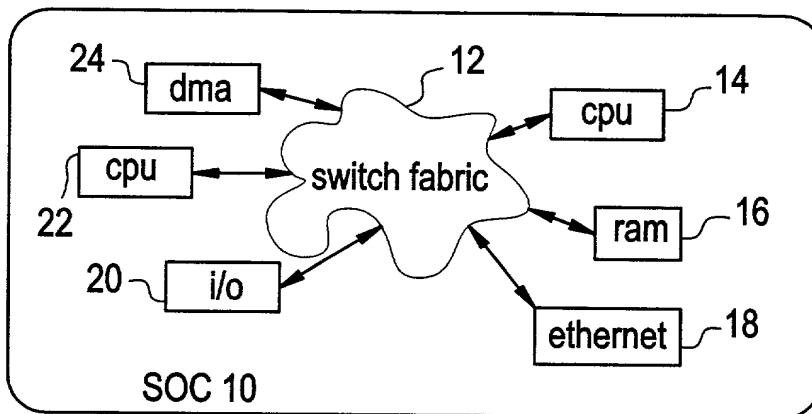


FIG. 2

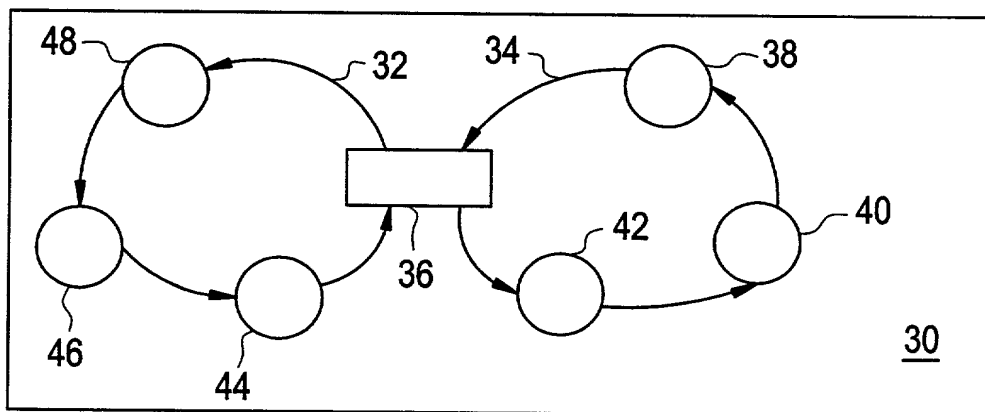


FIG. 3

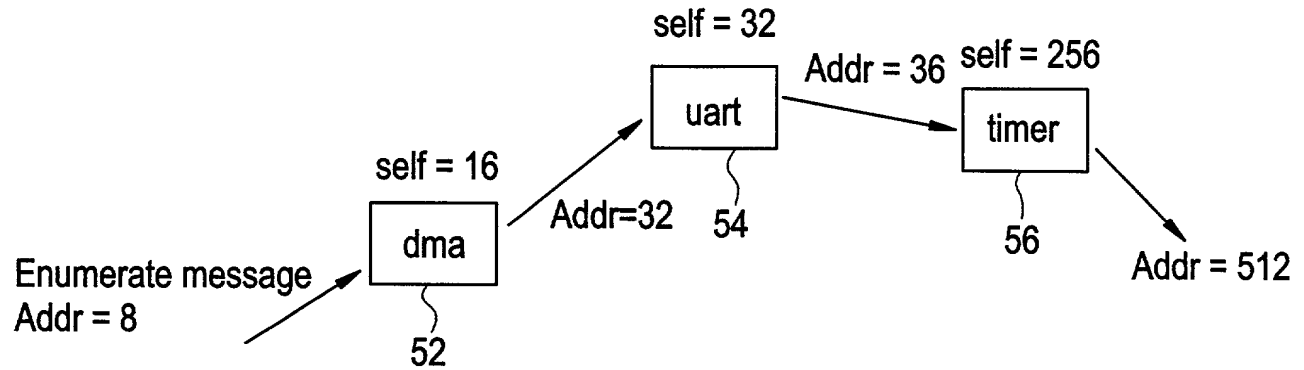


FIG. 4

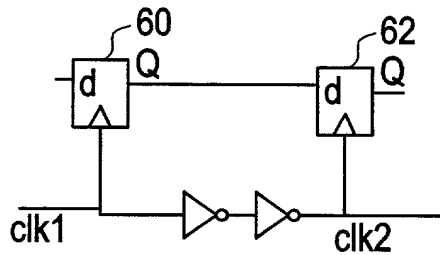


FIG. 5

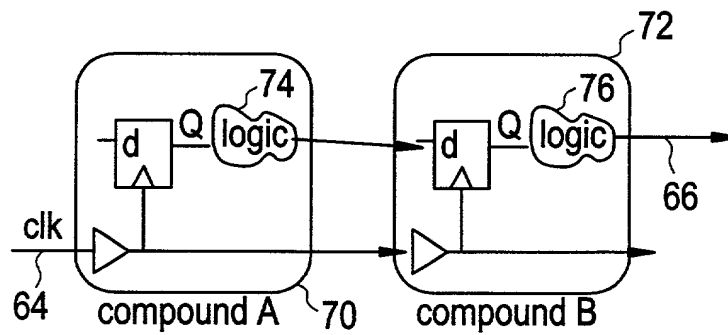


FIG. 6

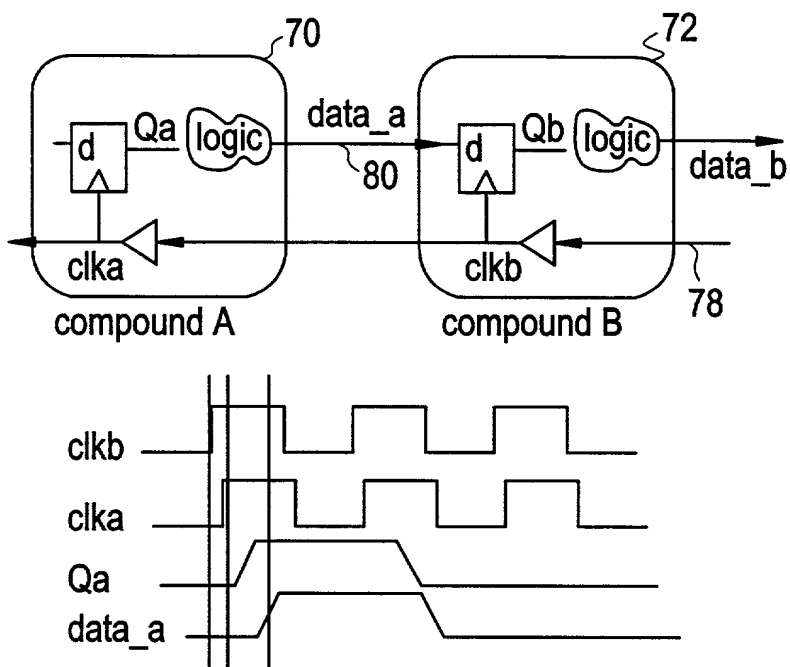


FIG. 7

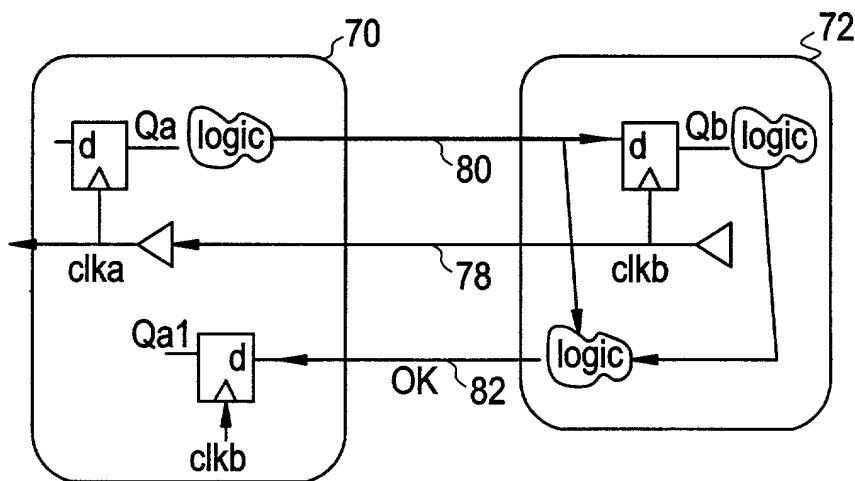


FIG. 8

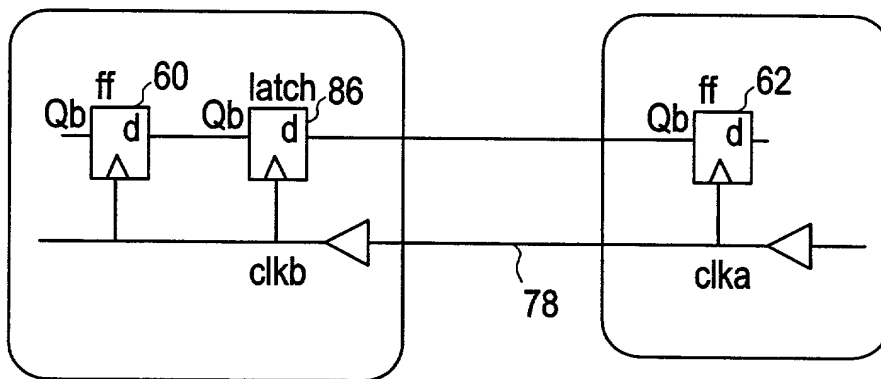


FIG. 9

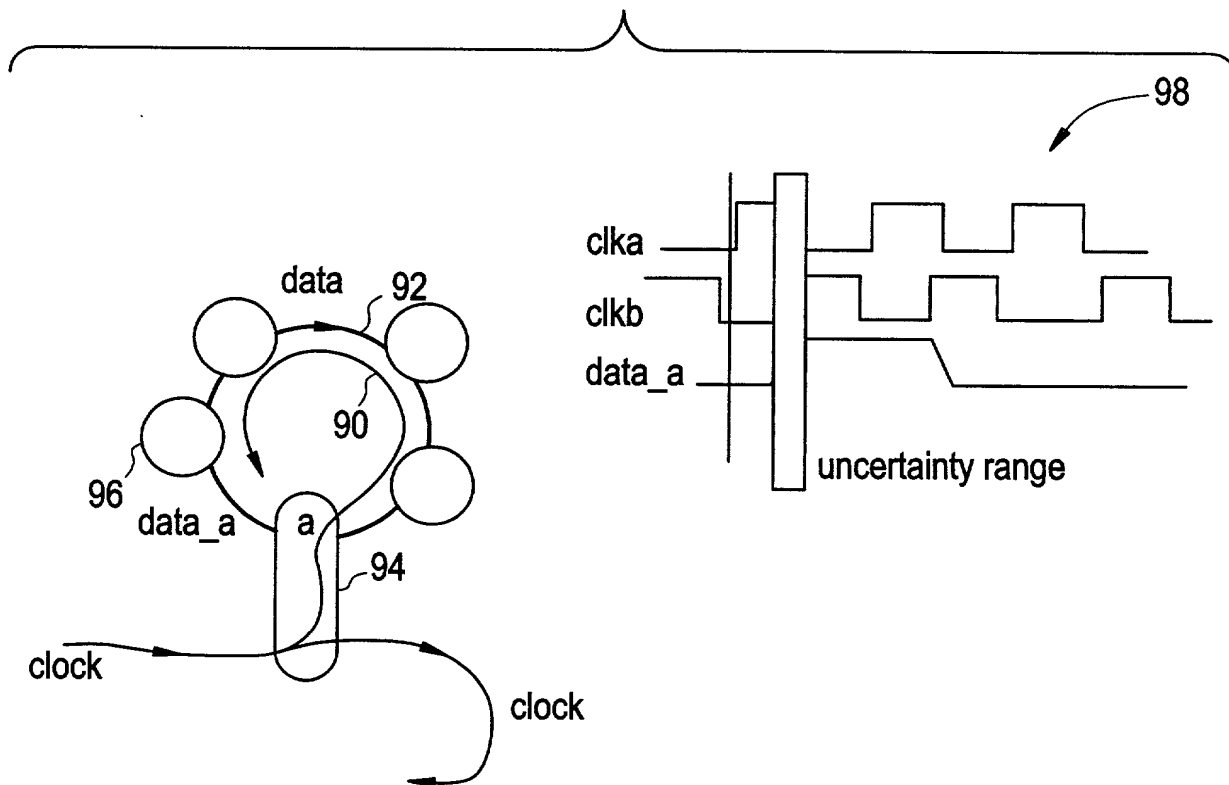


FIG. 14

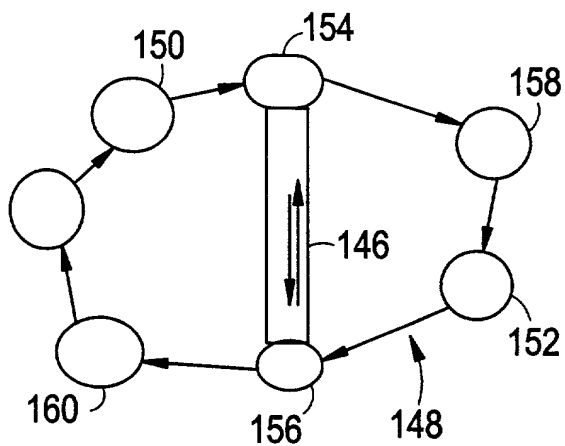


FIG. 15

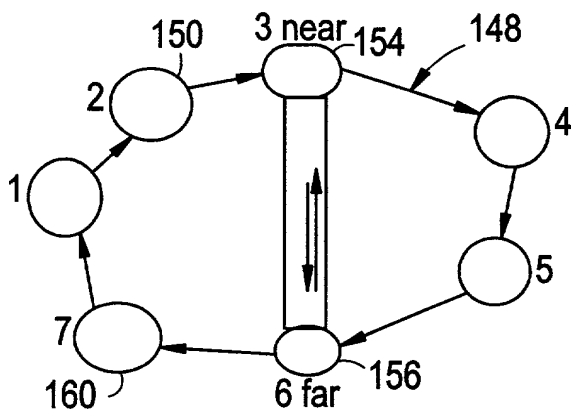


FIG. 16

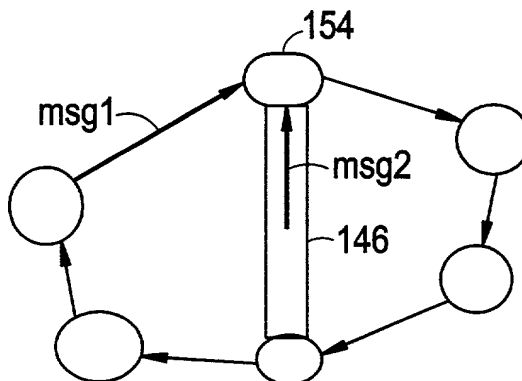


FIG. 17

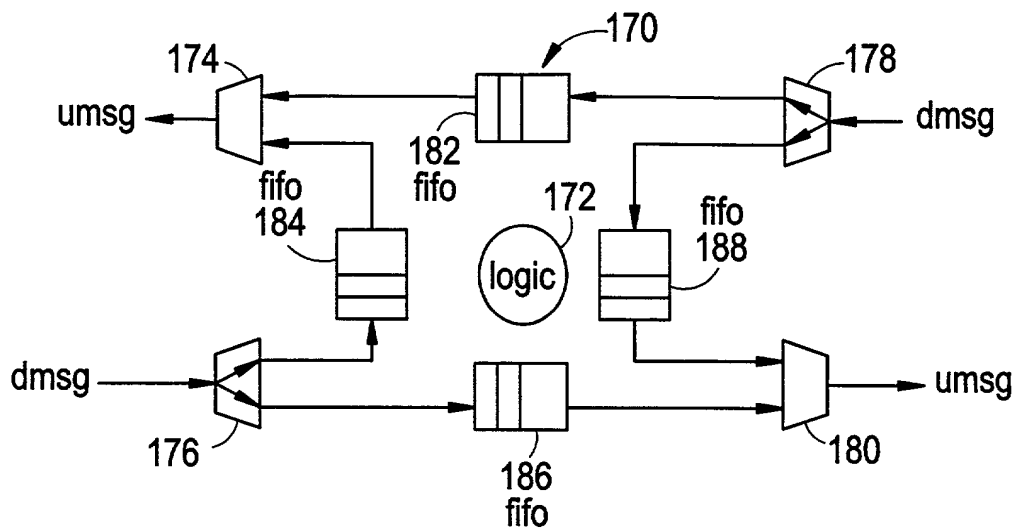


FIG. 18

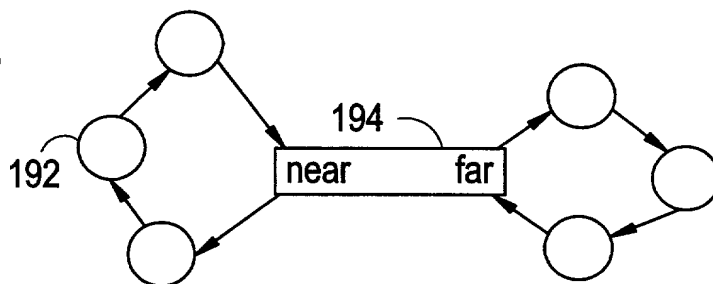


FIG. 19

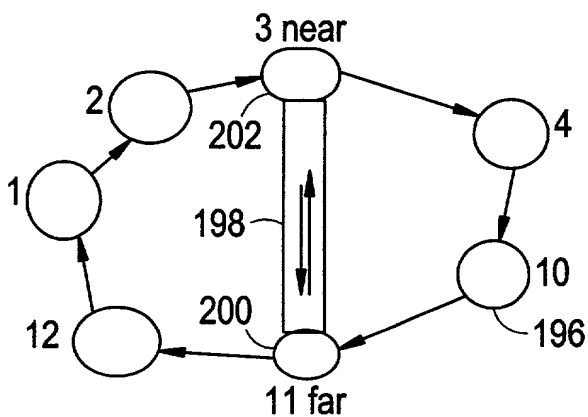


FIG. 20

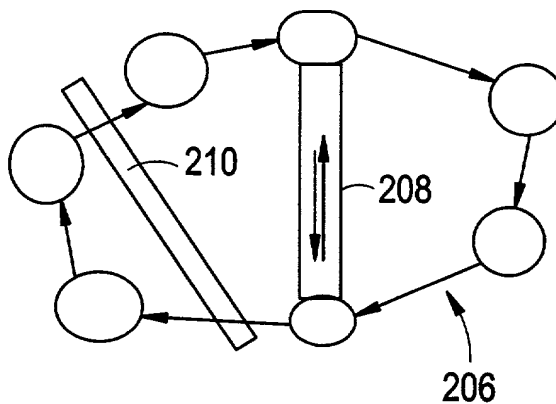


FIG. 21

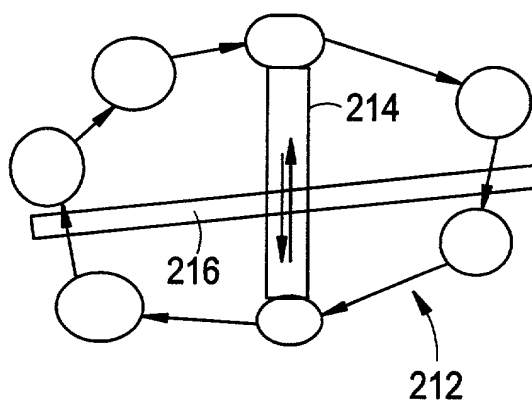


FIG. 22

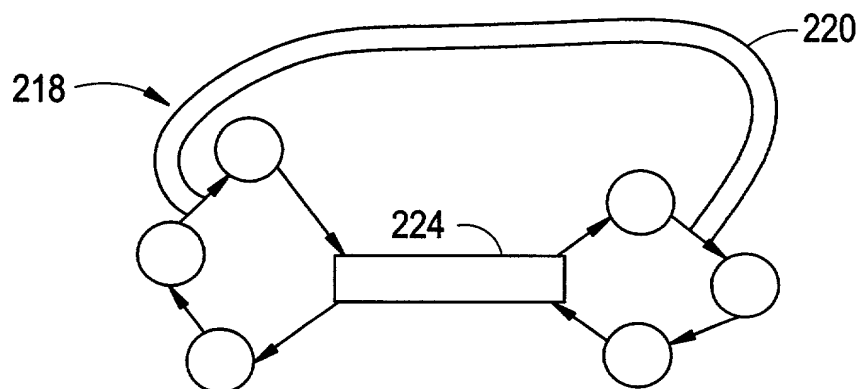


FIG. 23

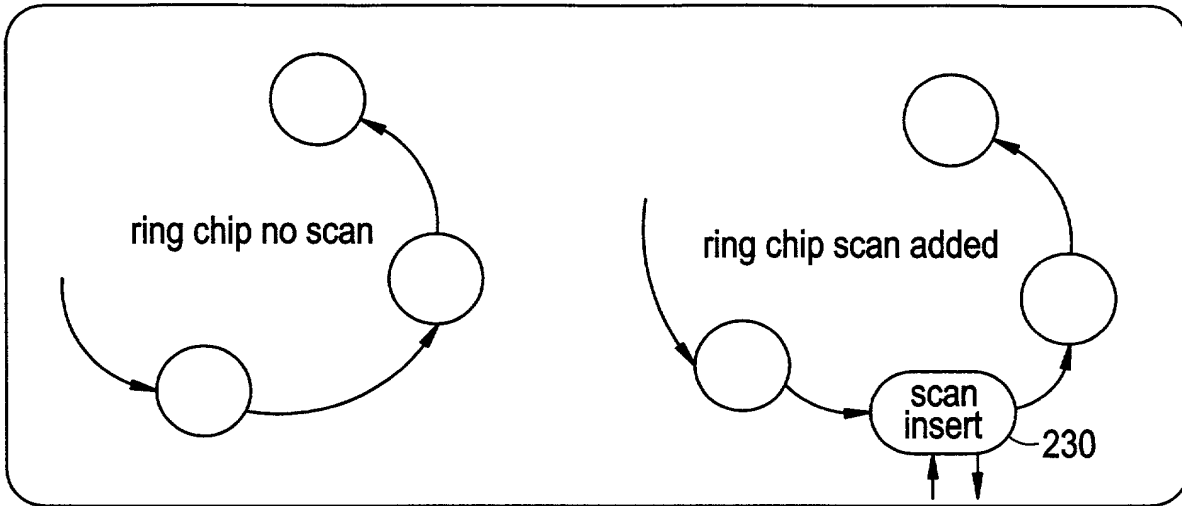


FIG. 24

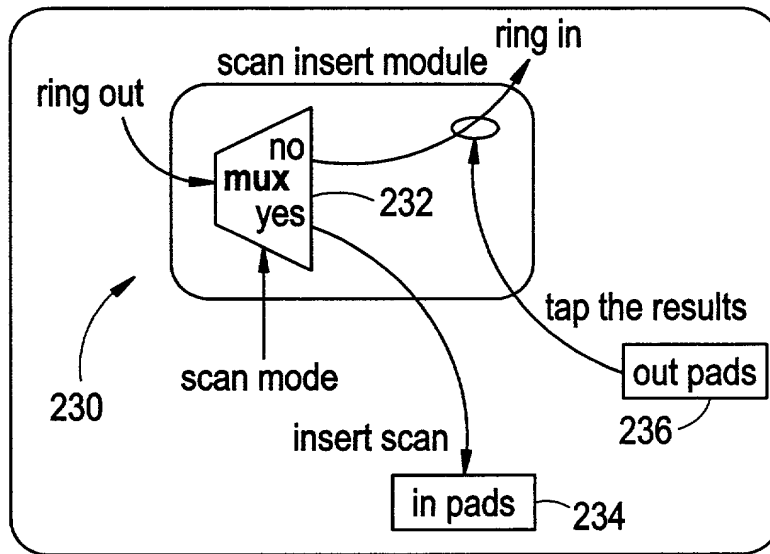


FIG. 25

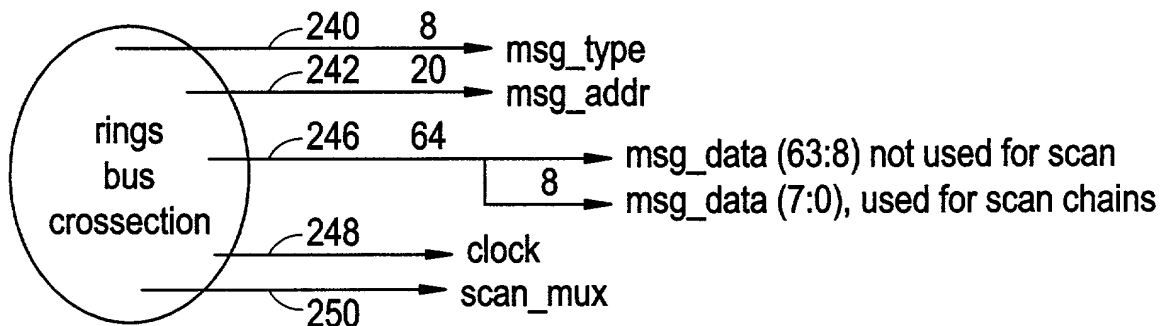


FIG. 26

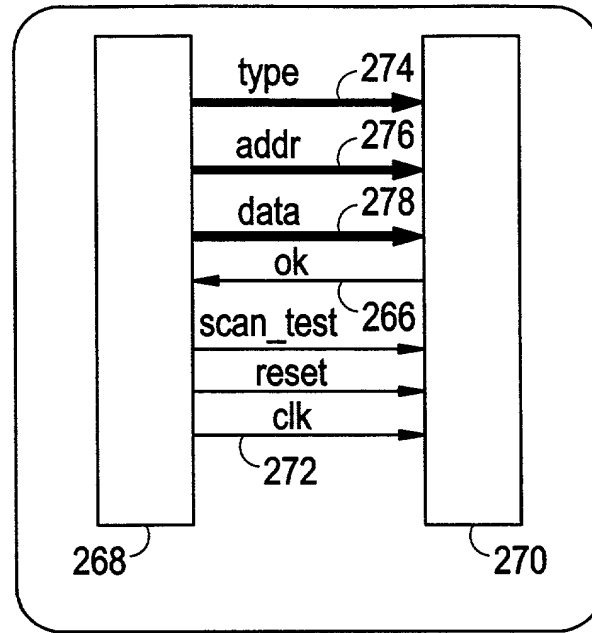


FIG. 27

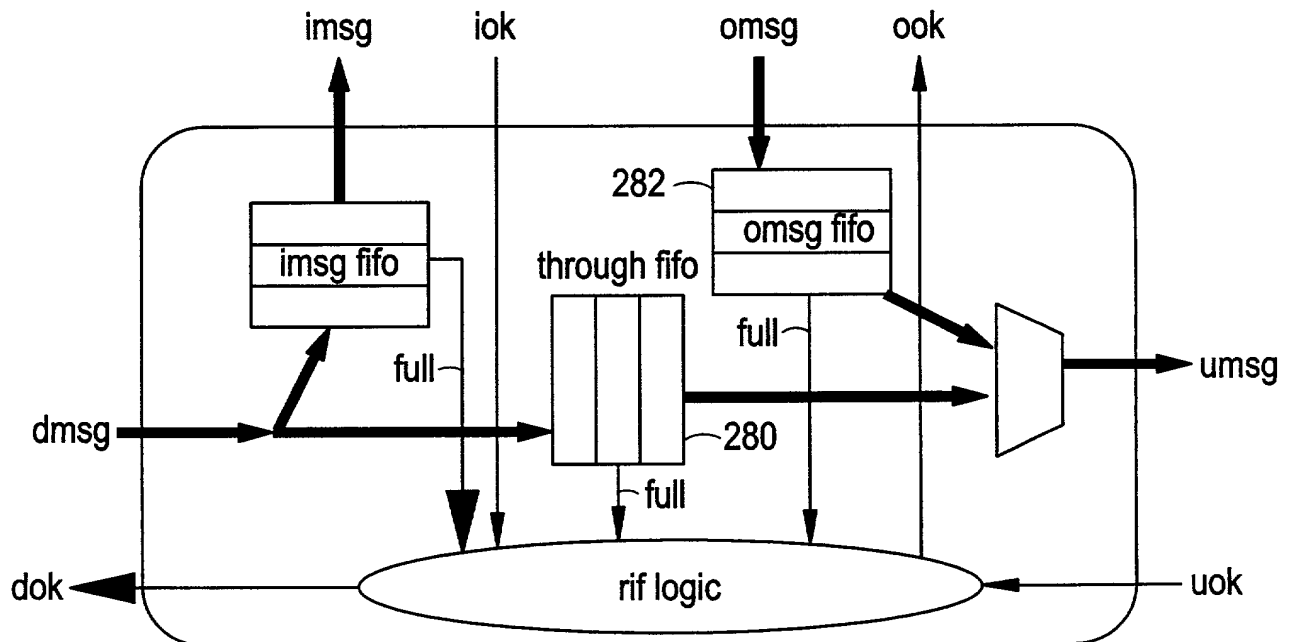


FIG. 28

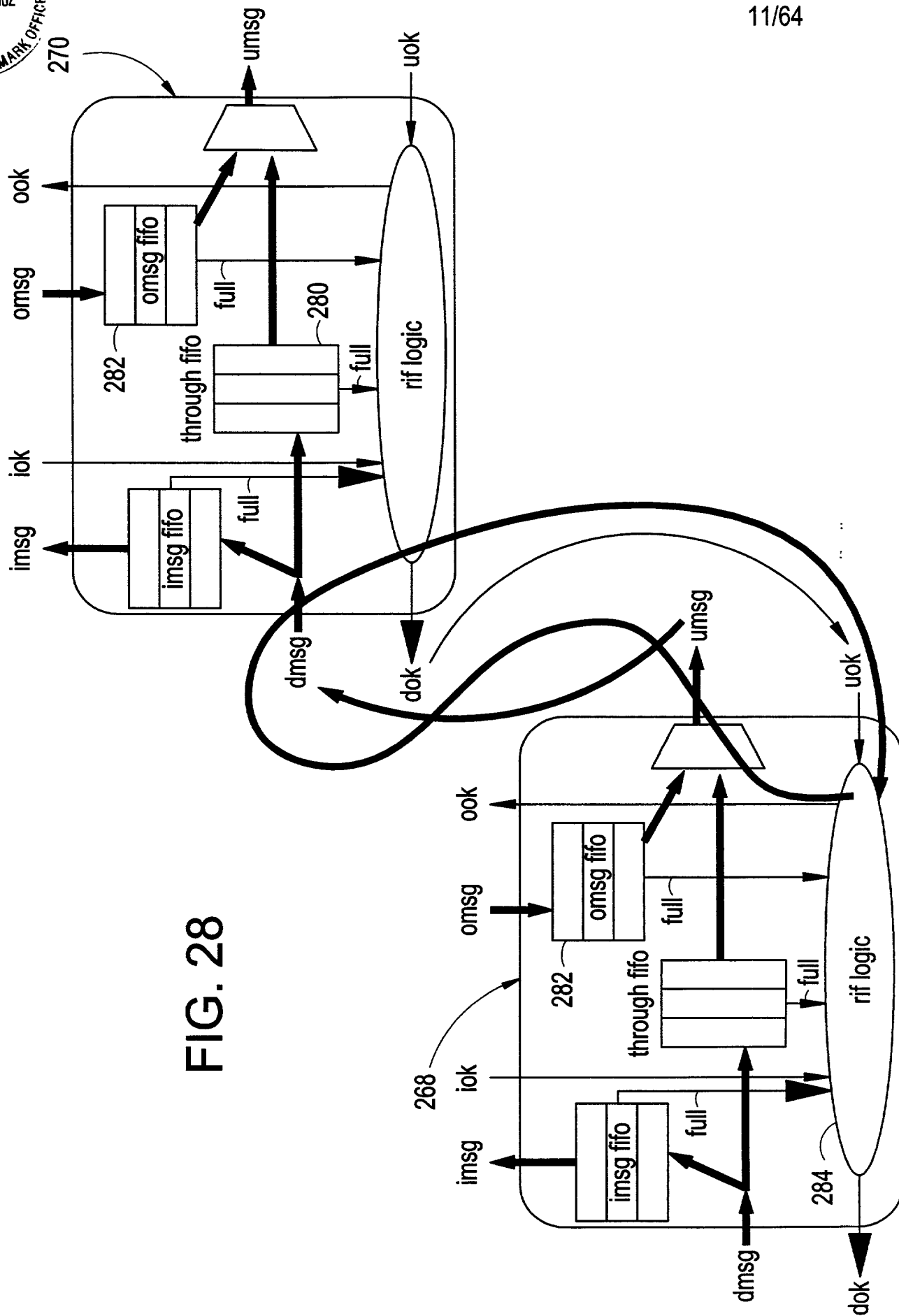


FIG. 29

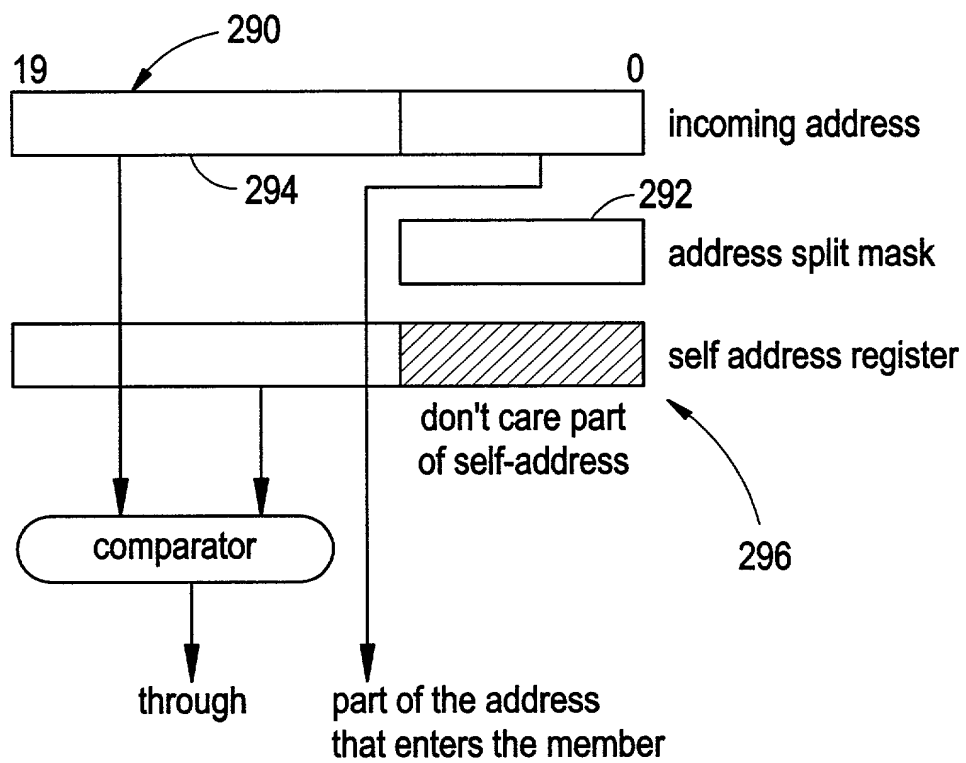


FIG. 30

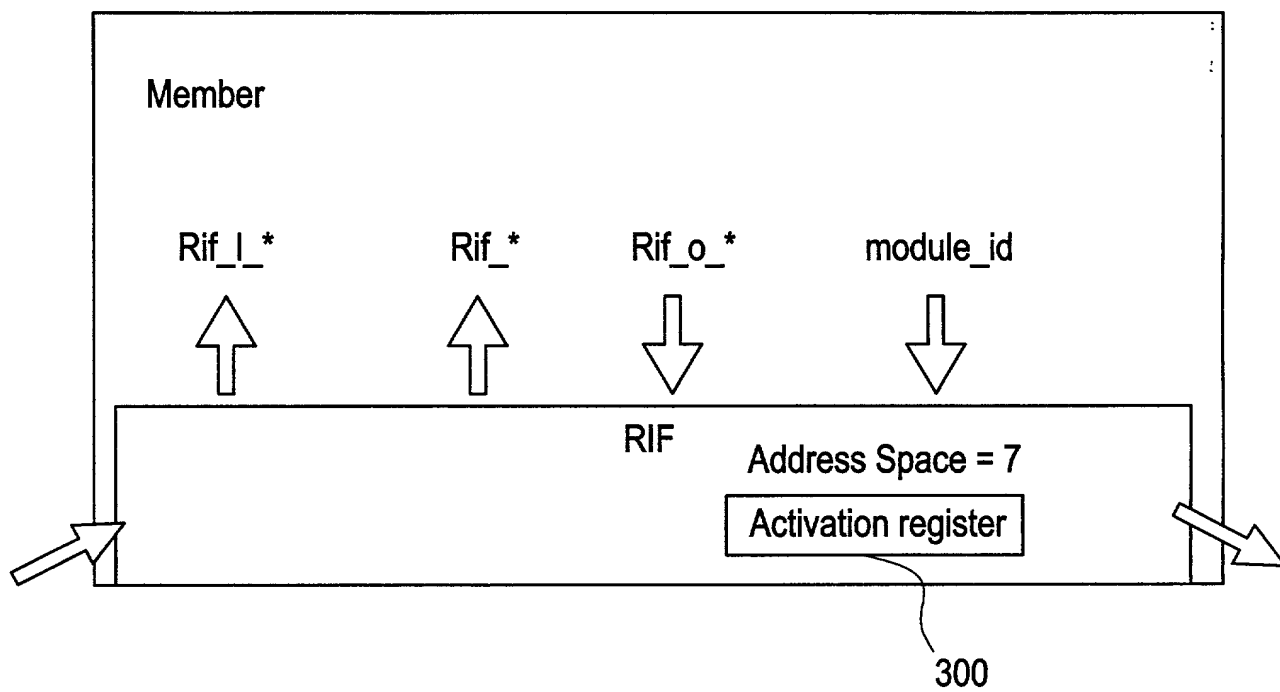


FIG. 31

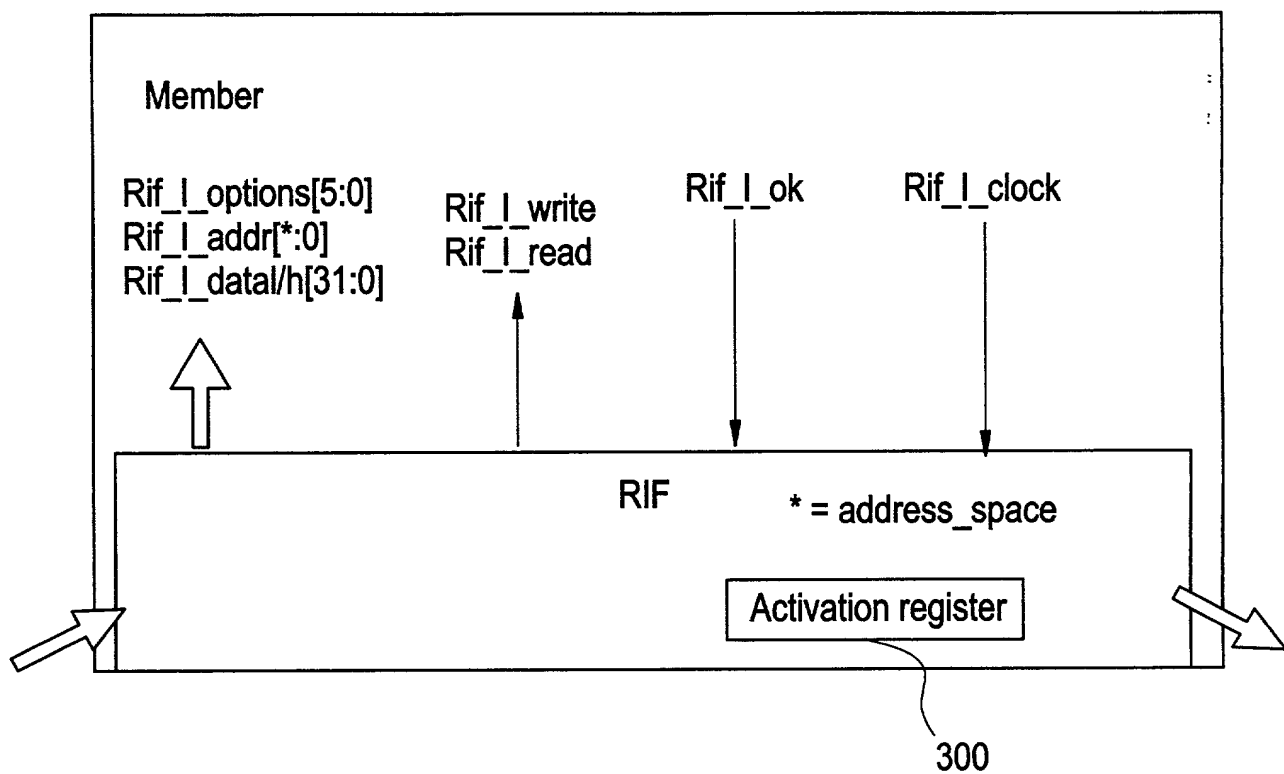


FIG. 32

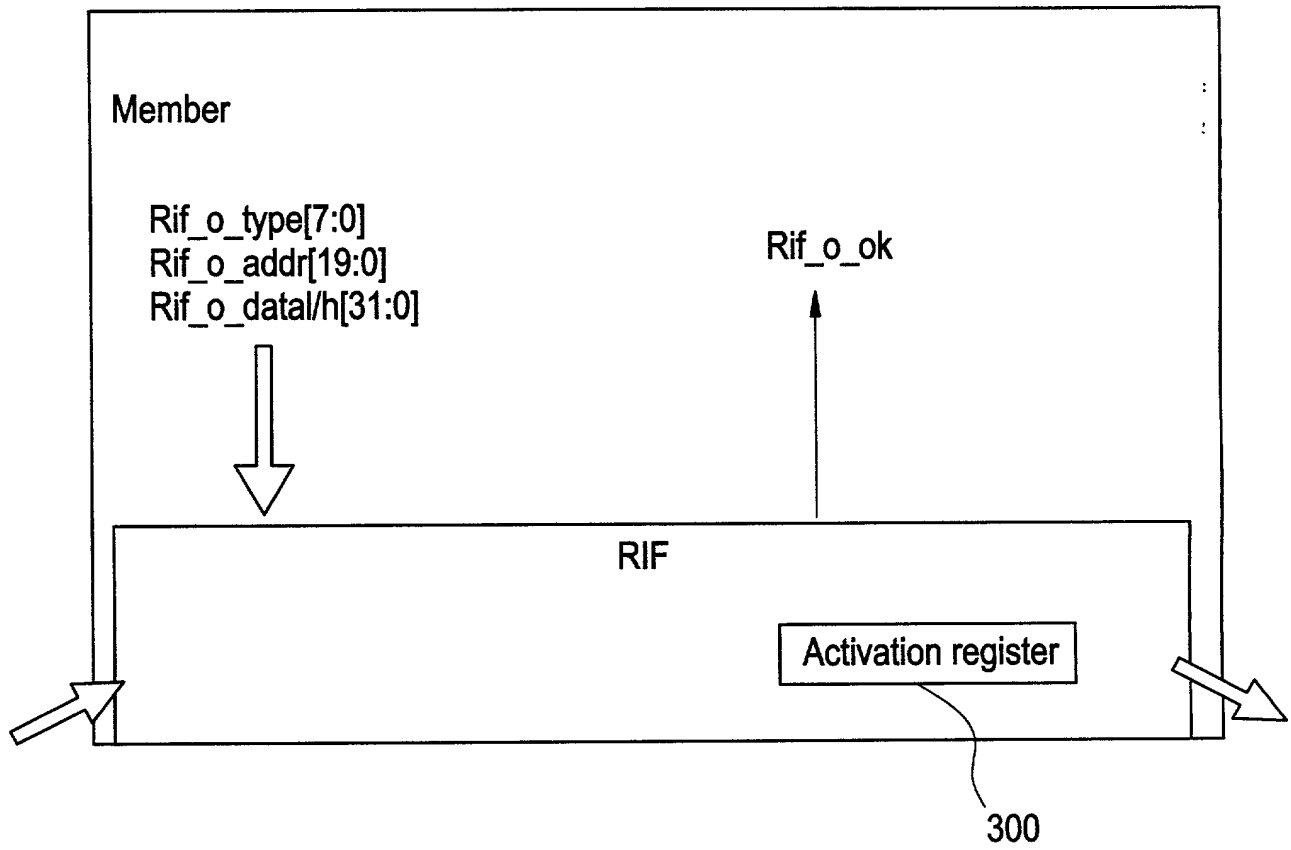


FIG. 33

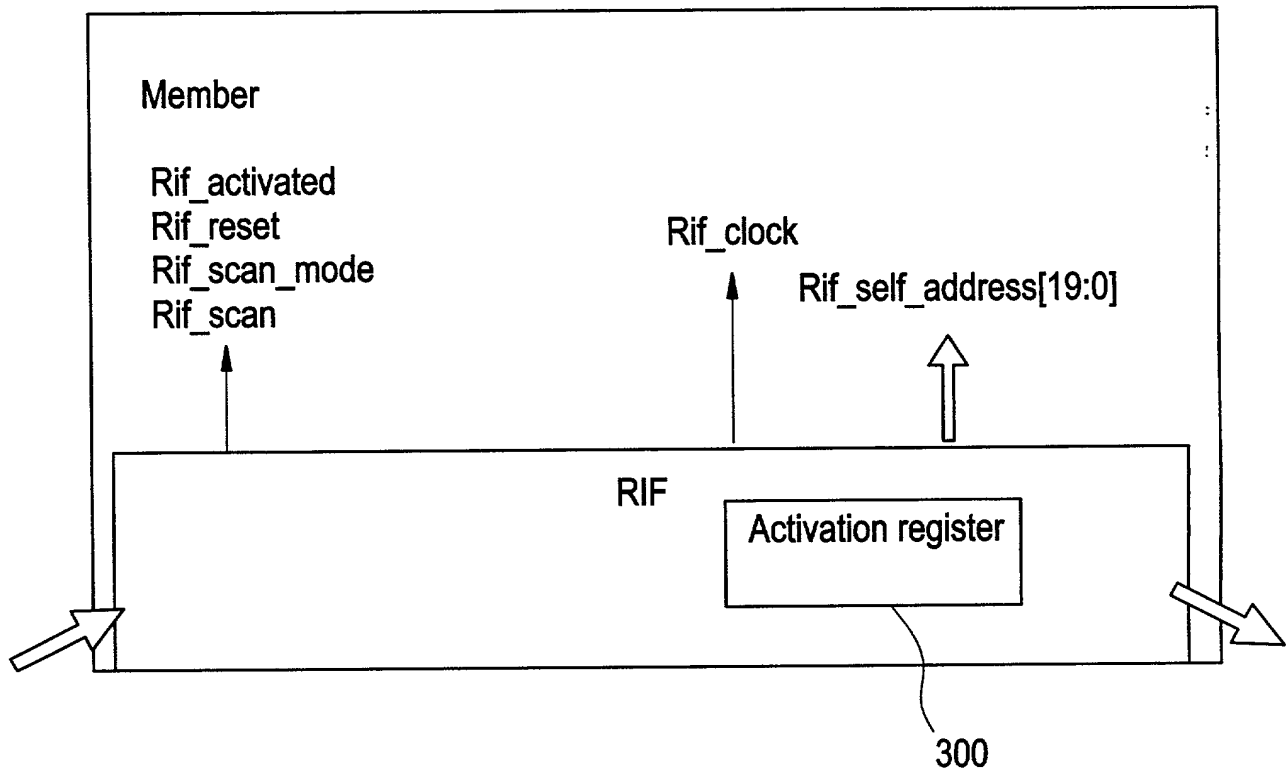


FIG. 34

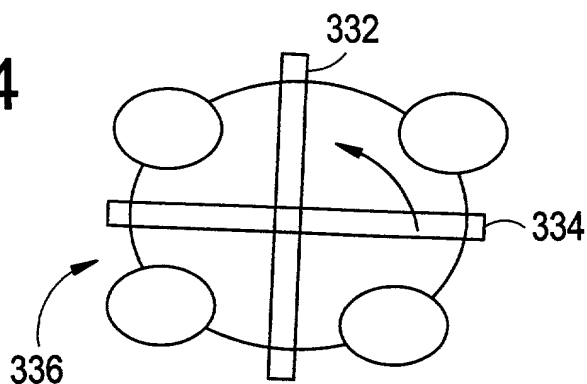


FIG. 35

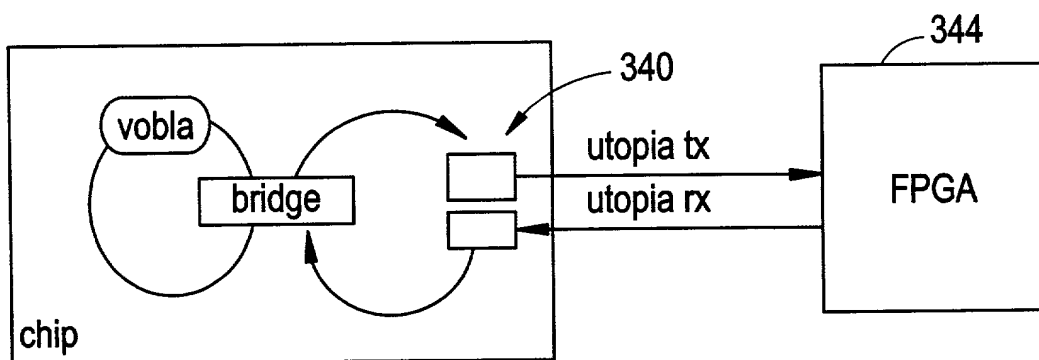


FIG. 36

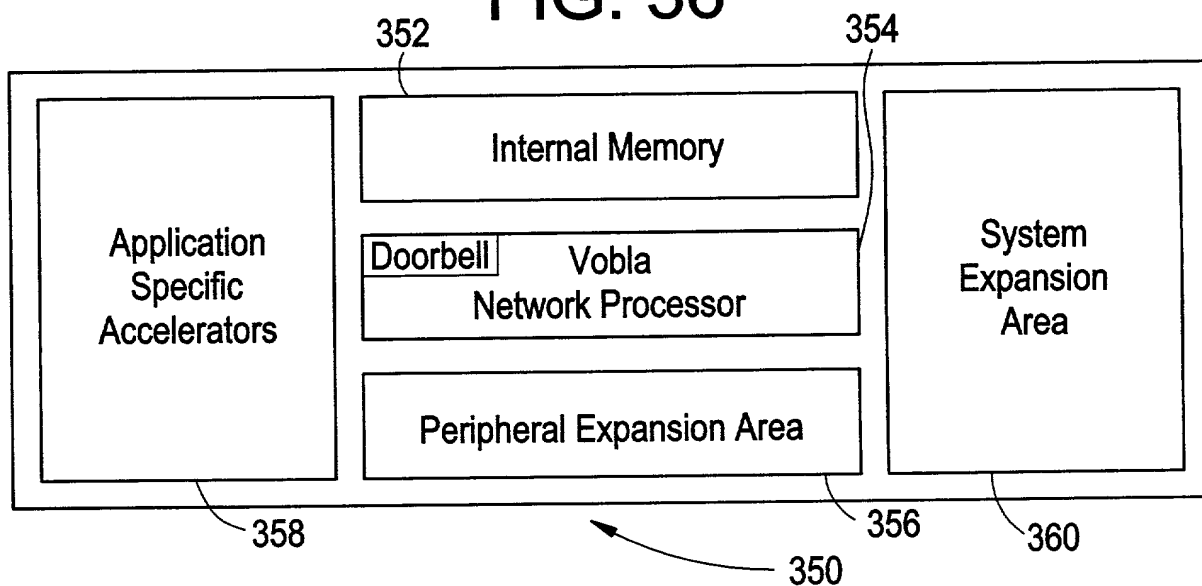
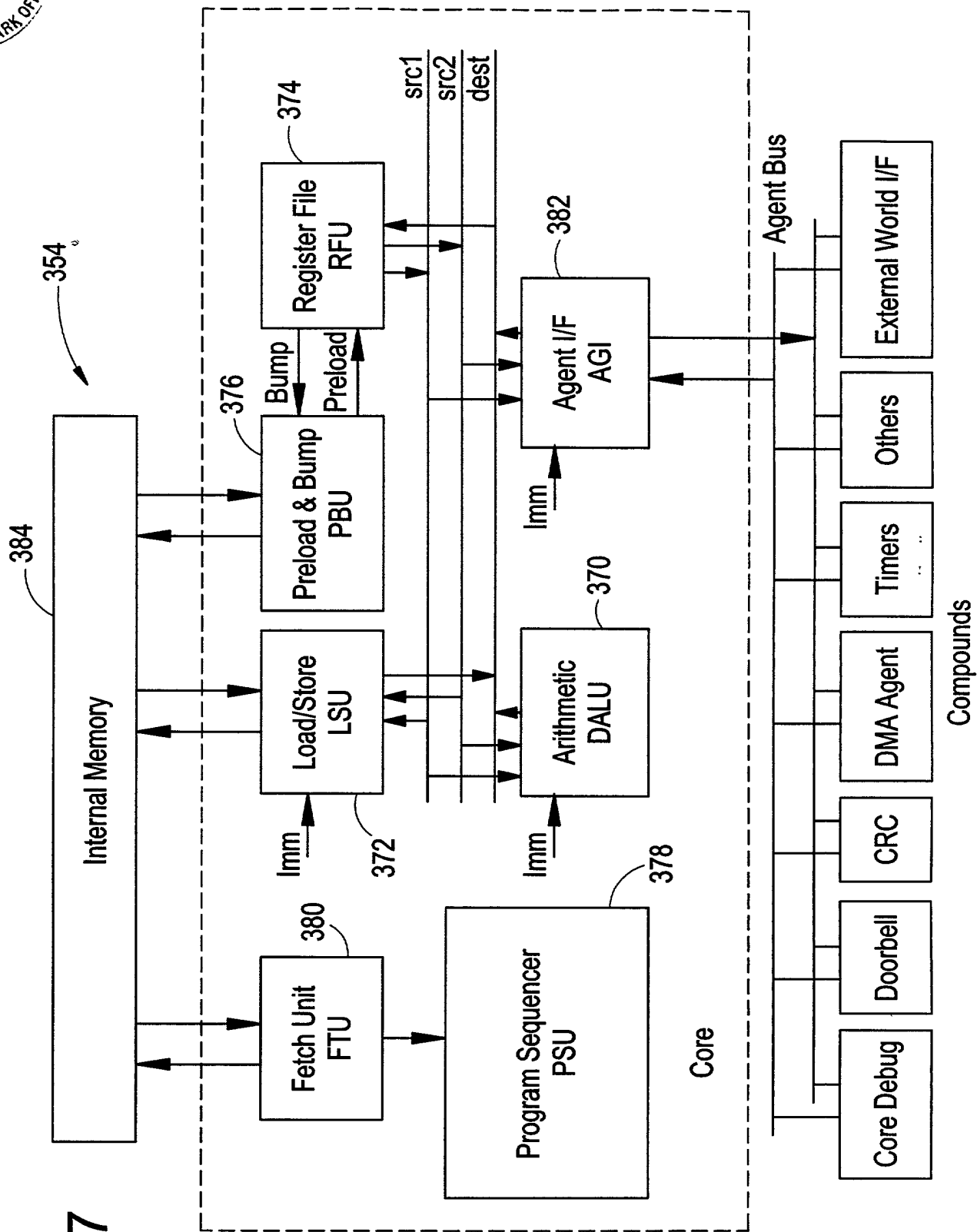


FIG. 37



Current Task (CTID)

Task_X

Next Task (NTID)

Task_Y

Logic

To Memory

Write Queue

Logic

Memory

Destination

Preload regs of Task_Y

Tag

Active (Active Reg. File)

Shadow 1 (Active Shadow)

Shadow 2 (Preload Shadow)

hit/miss Source

H Mux

Source Operand of Task_X

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After a task switch

Current Task (CTID)

Task_Y

Next Task (NTID)

Task_Z

Logic

To Memory

Write Queue

Logic

Memory

Destination

Preload regs of Task_Z

Tag

Active (Active Reg. File)

Shadow 1 (Active Shadow)

Shadow 2 (Preload Shadow)

hit/miss of Source

H Mux

Source Operand of Task_Y

392

10043309200

FIG. 39

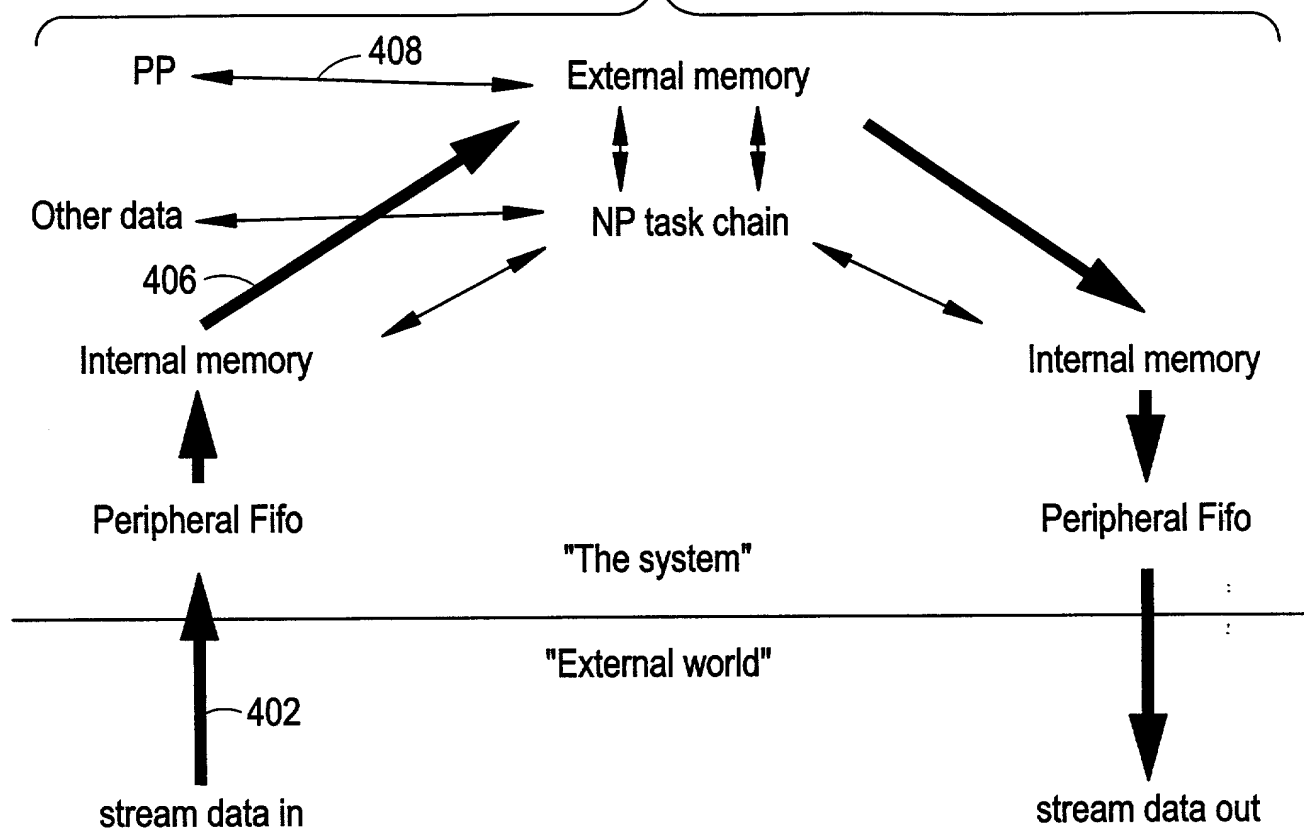


FIG. 40

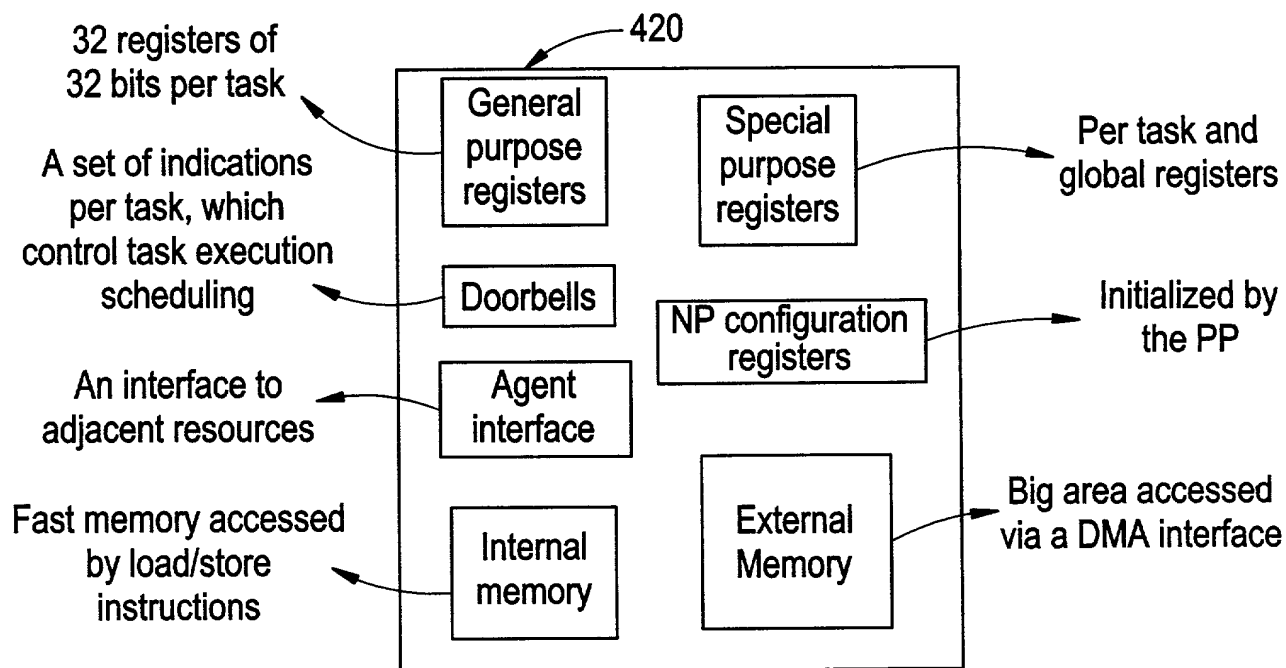


FIG. 41

R1 register

3 3 2 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0



s - sticky bit
 eq - equal/zero
 lt - less then/negative
 gt - greater then/positive
 c - carry
 mb - reflection of the RAM mult-reader busy indication

FIG. 42

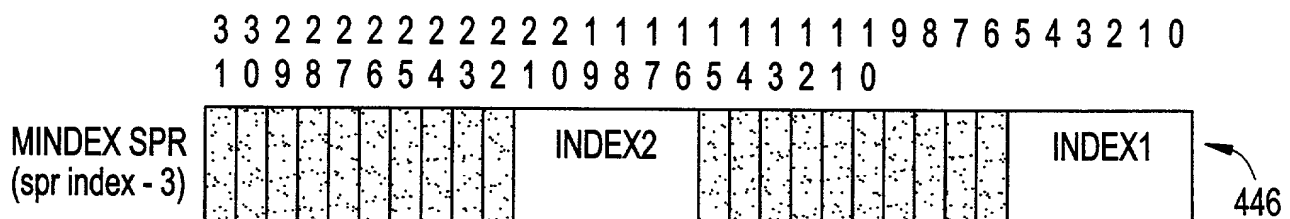
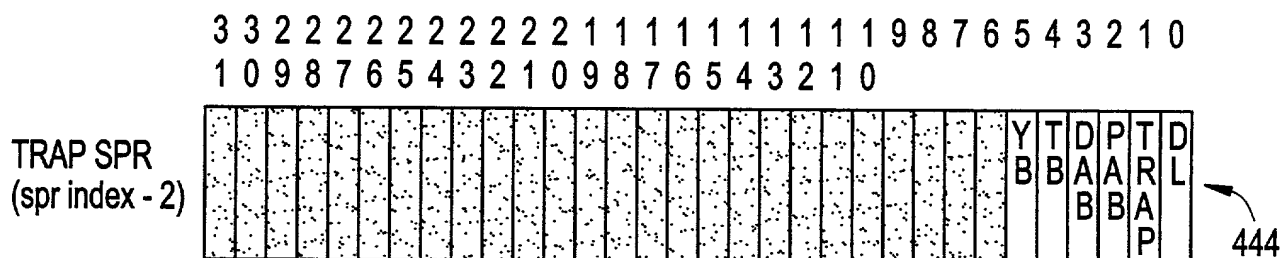
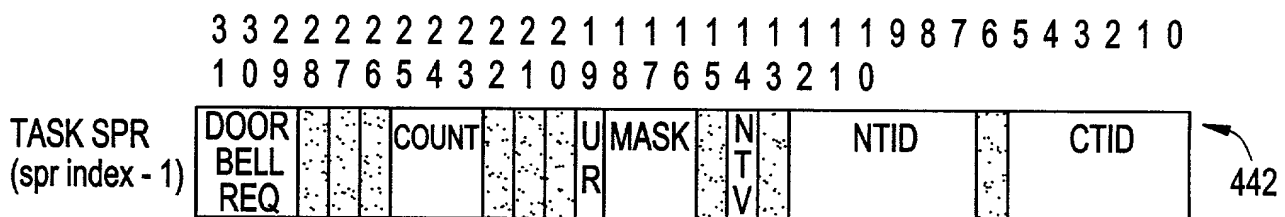
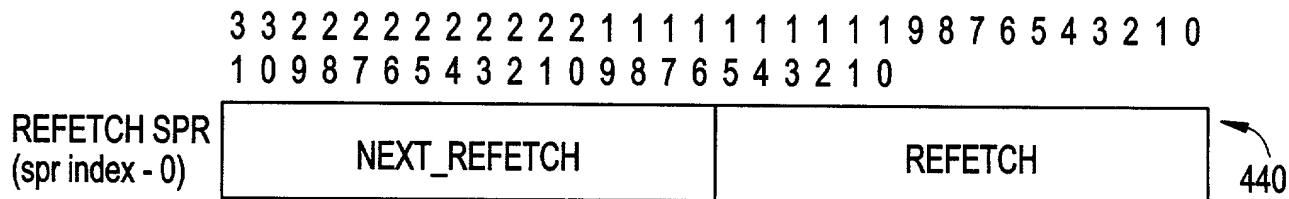


FIG. 43

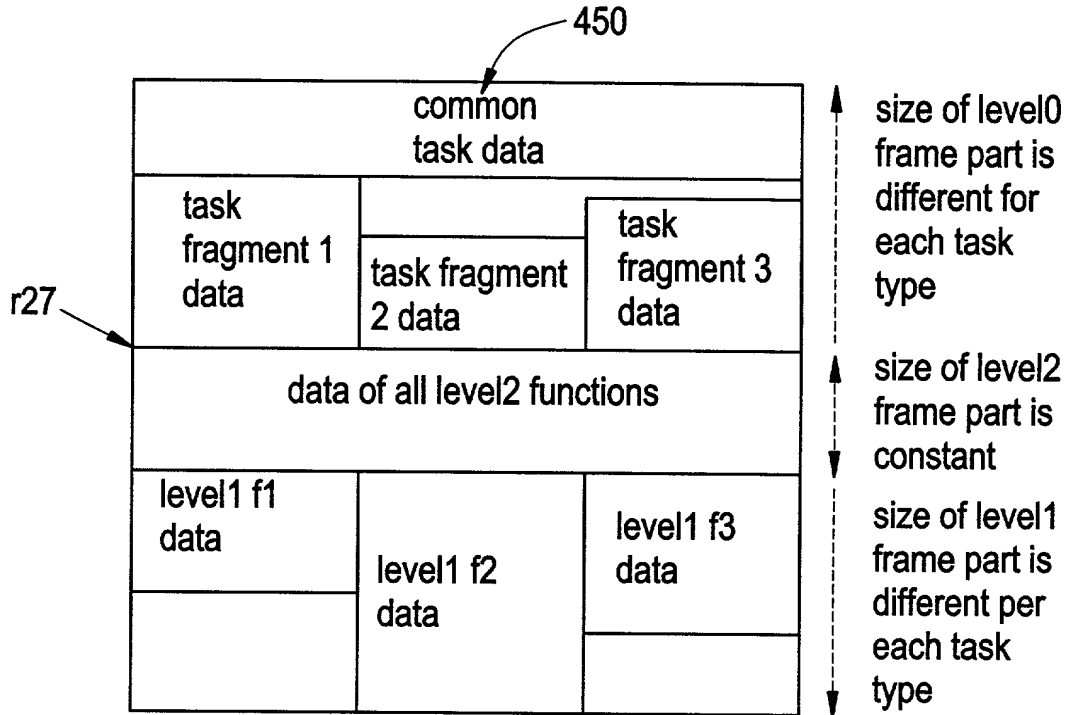


FIG. 44

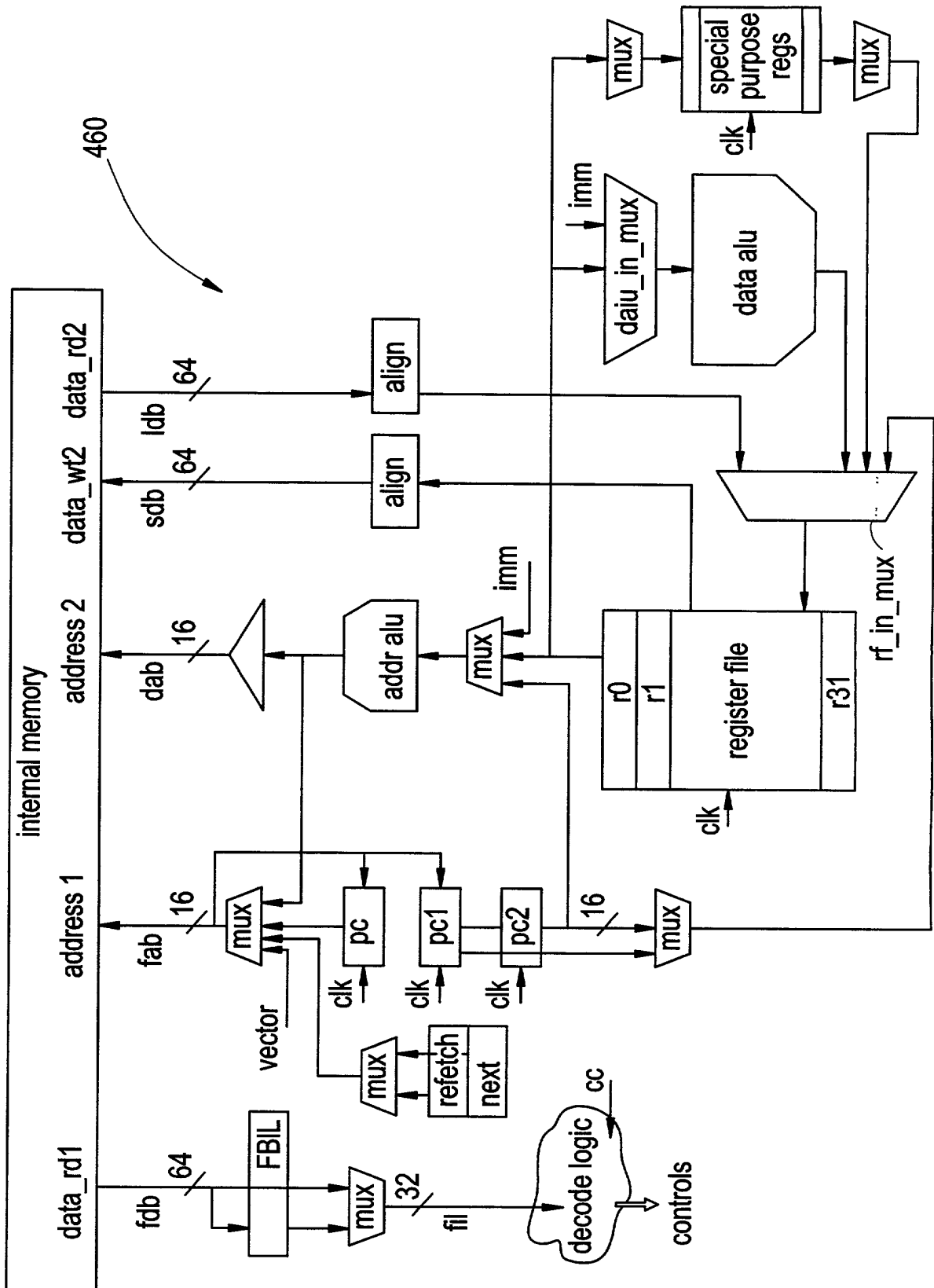
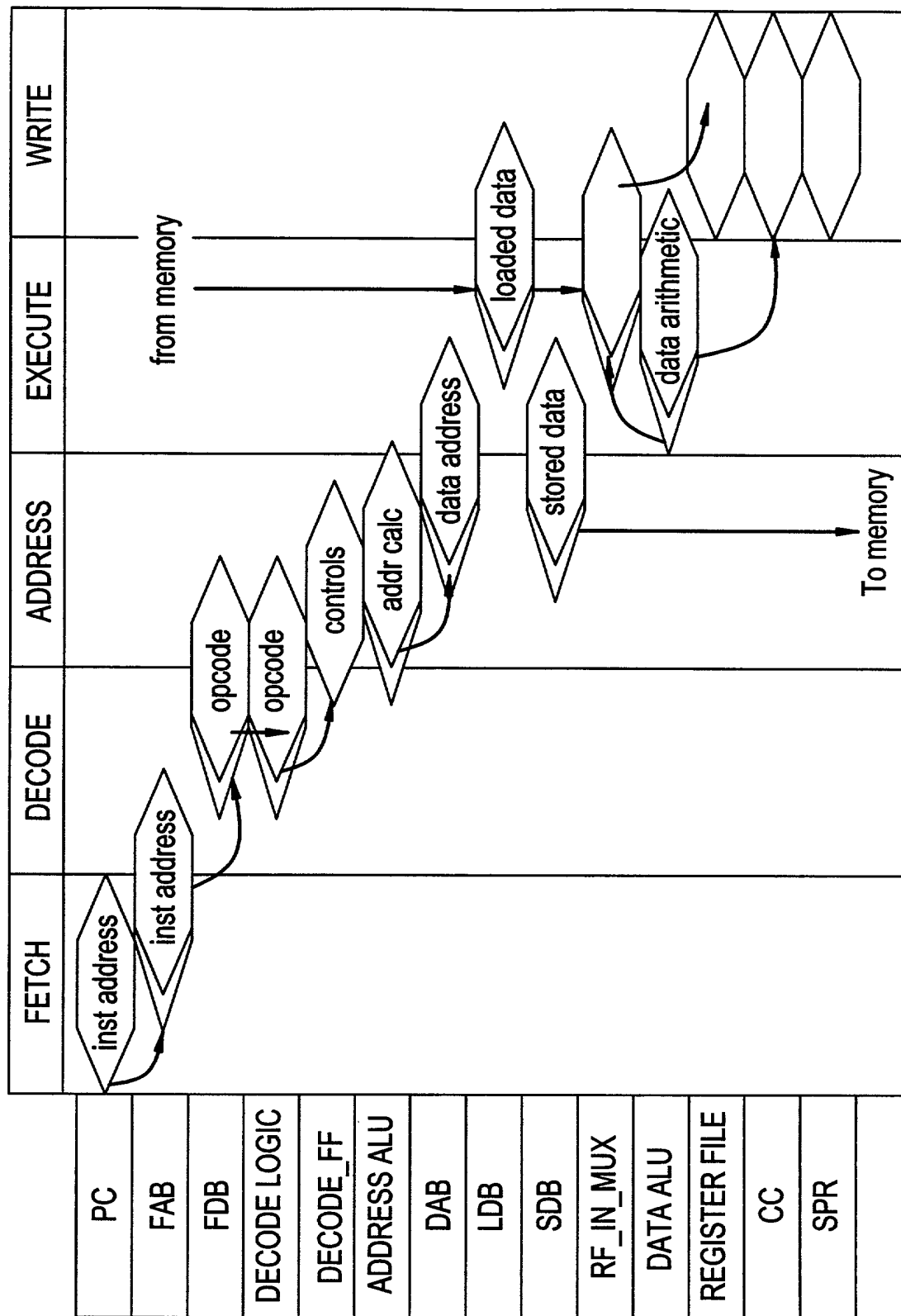


FIG. 45



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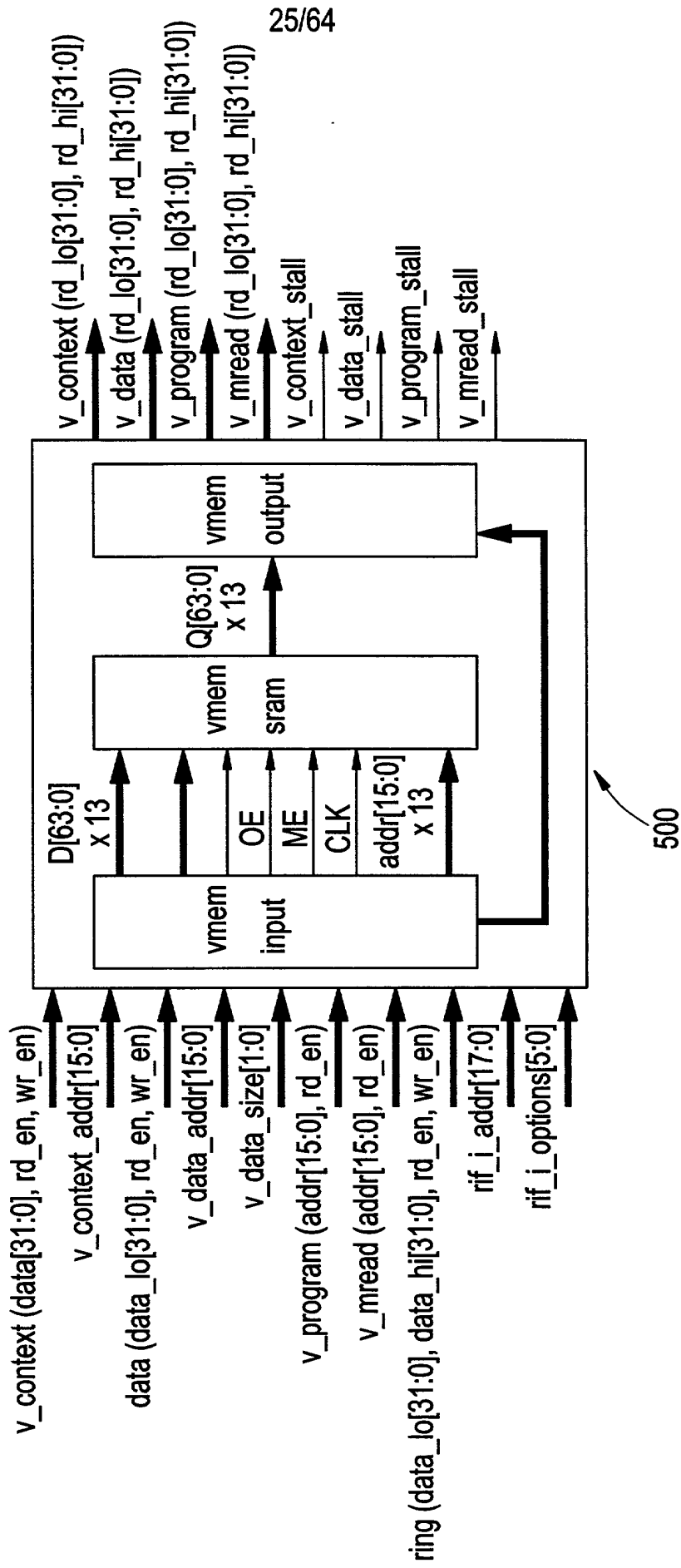


FIG. 47

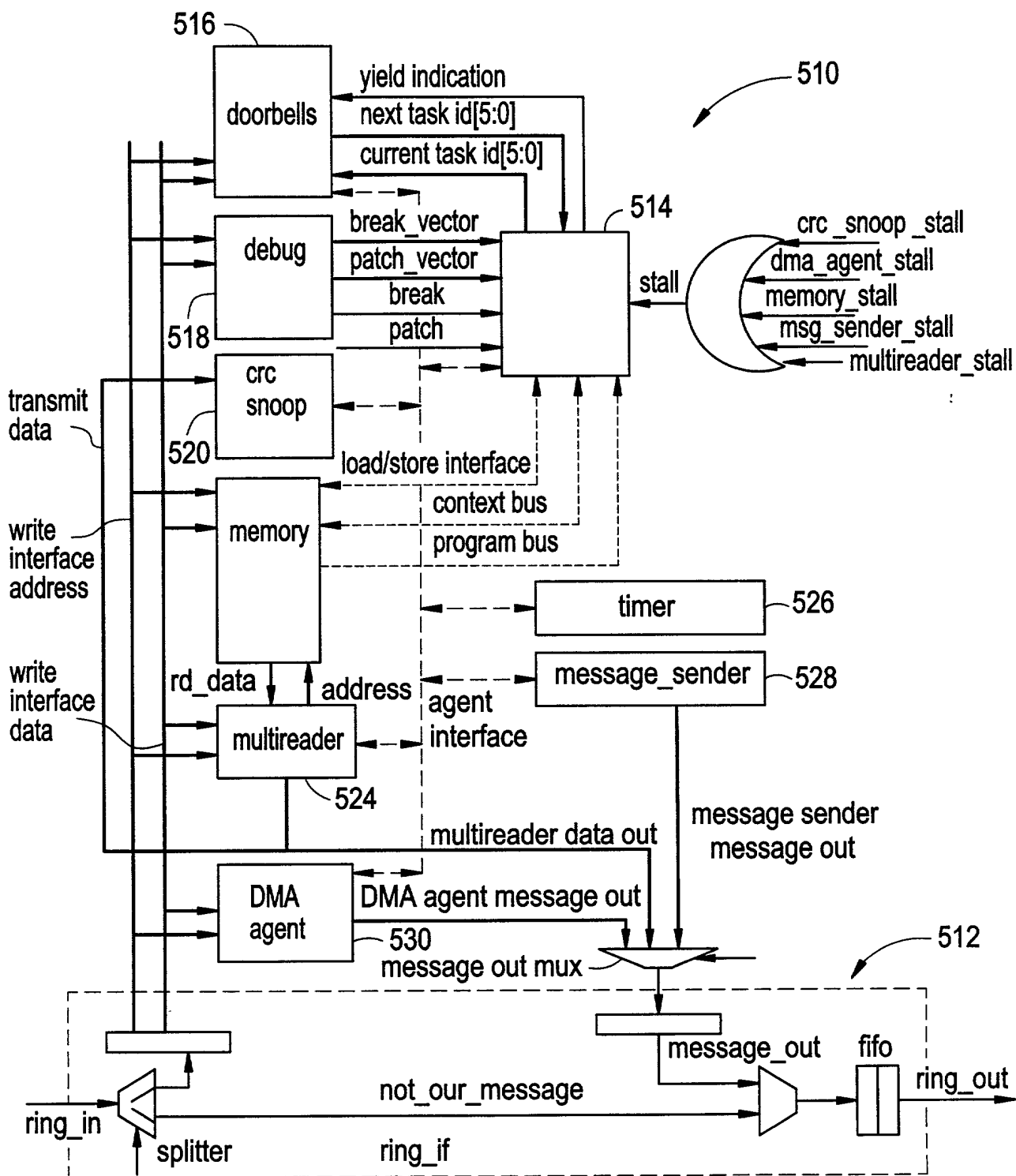


FIG. 48

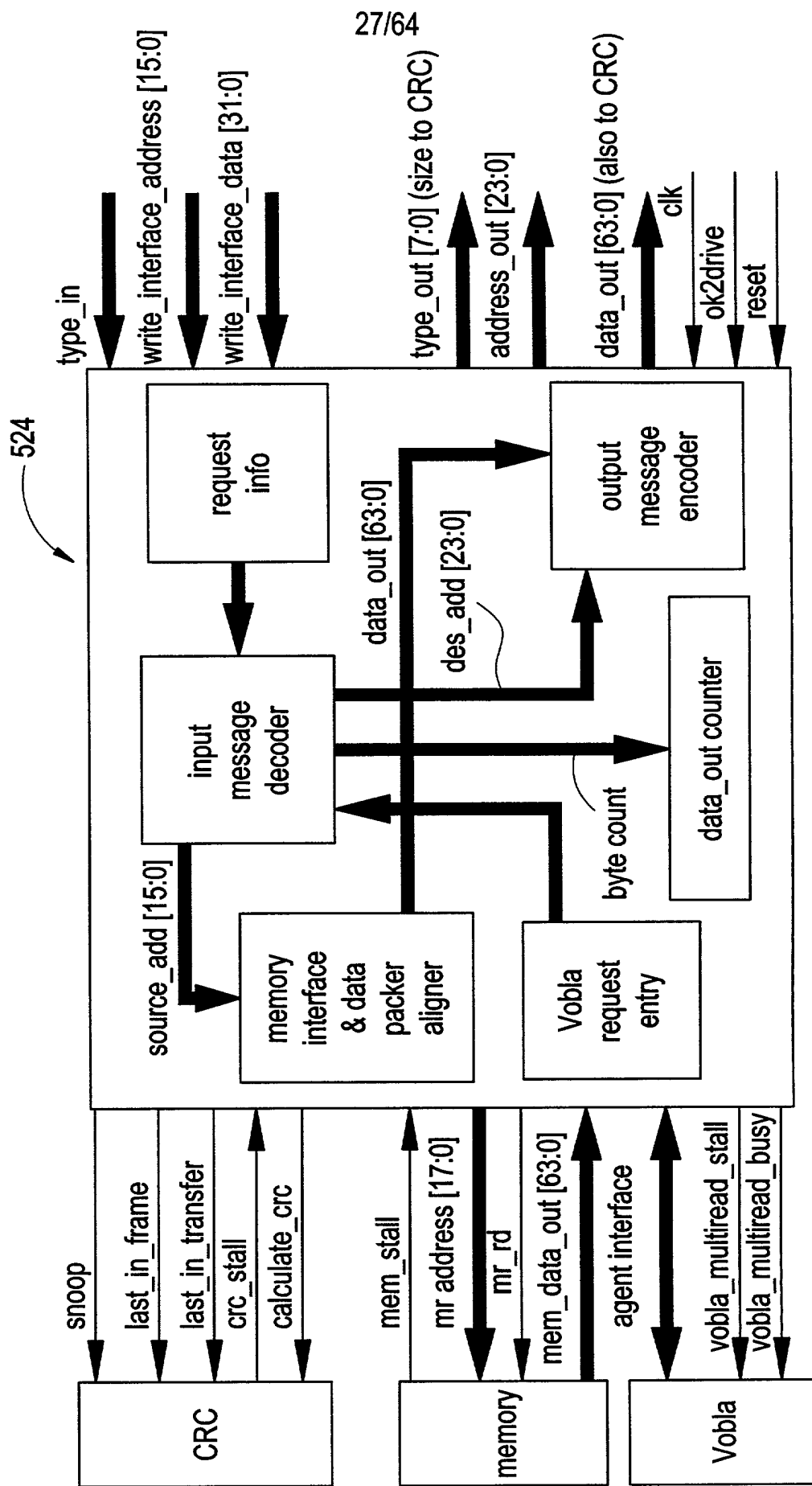


FIG. 49

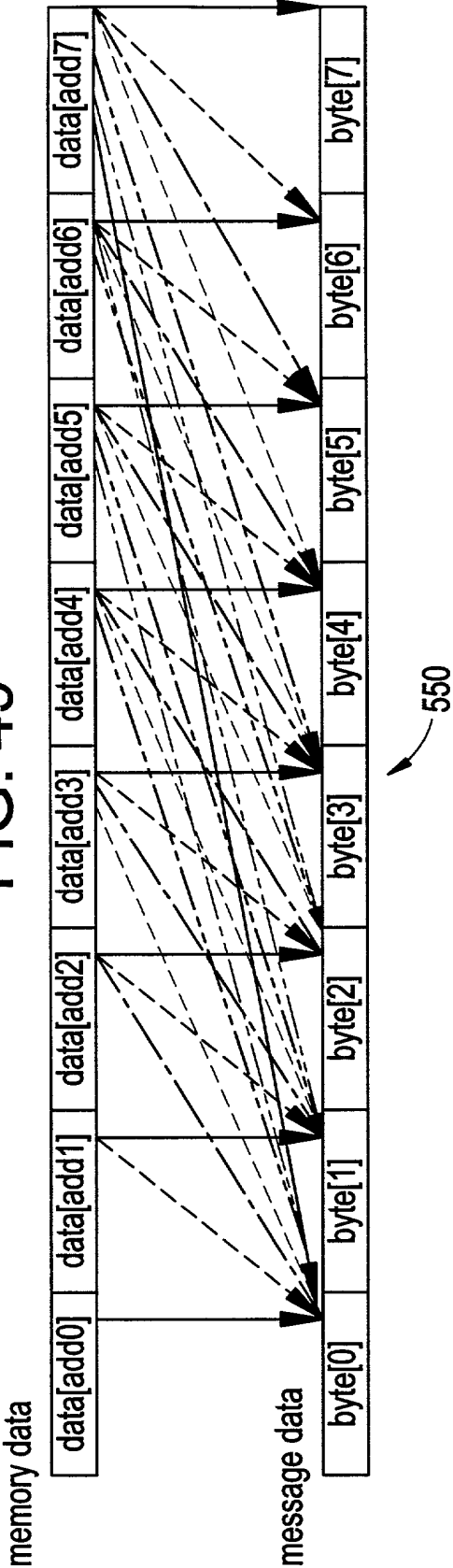


FIG. 50

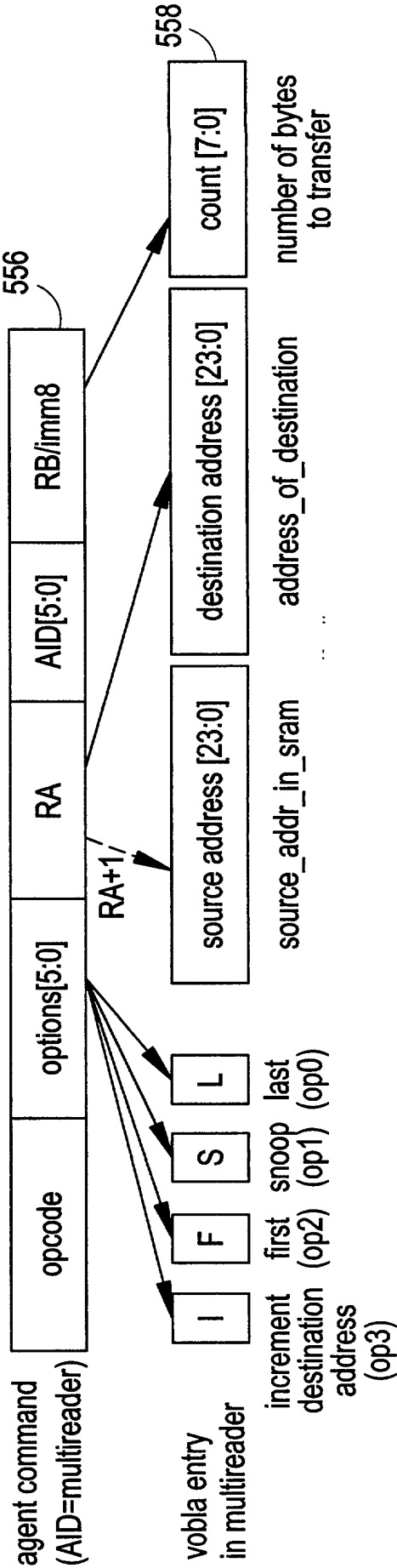


FIG. 51

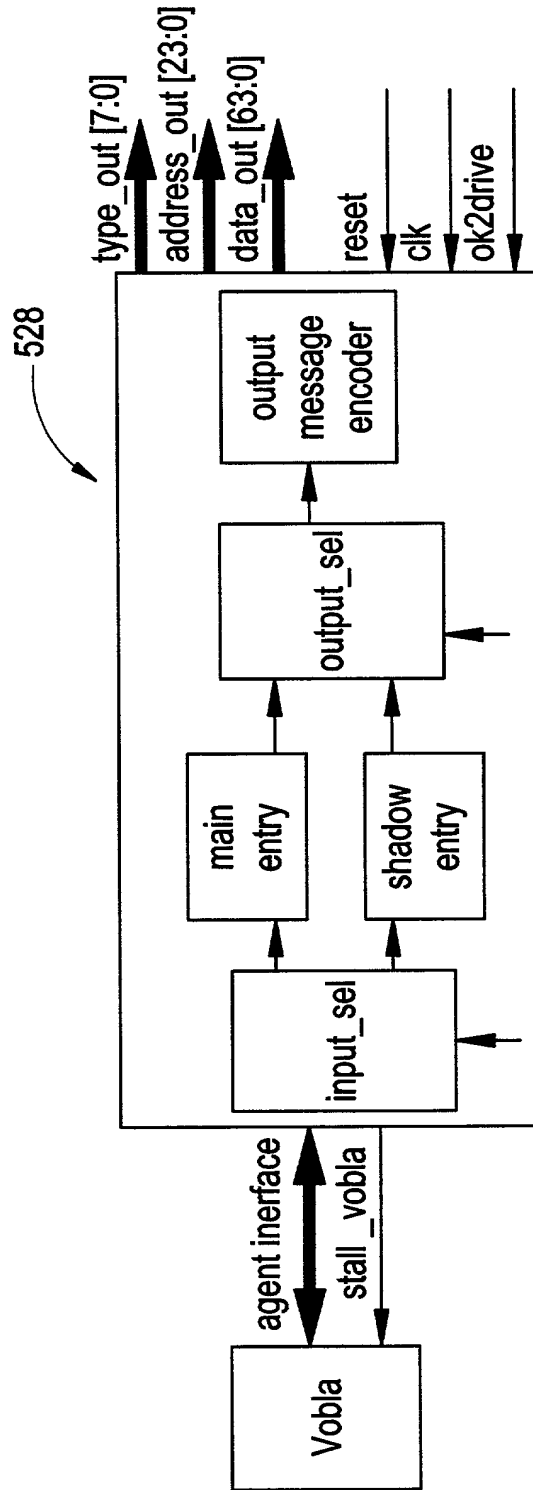


FIG. 52

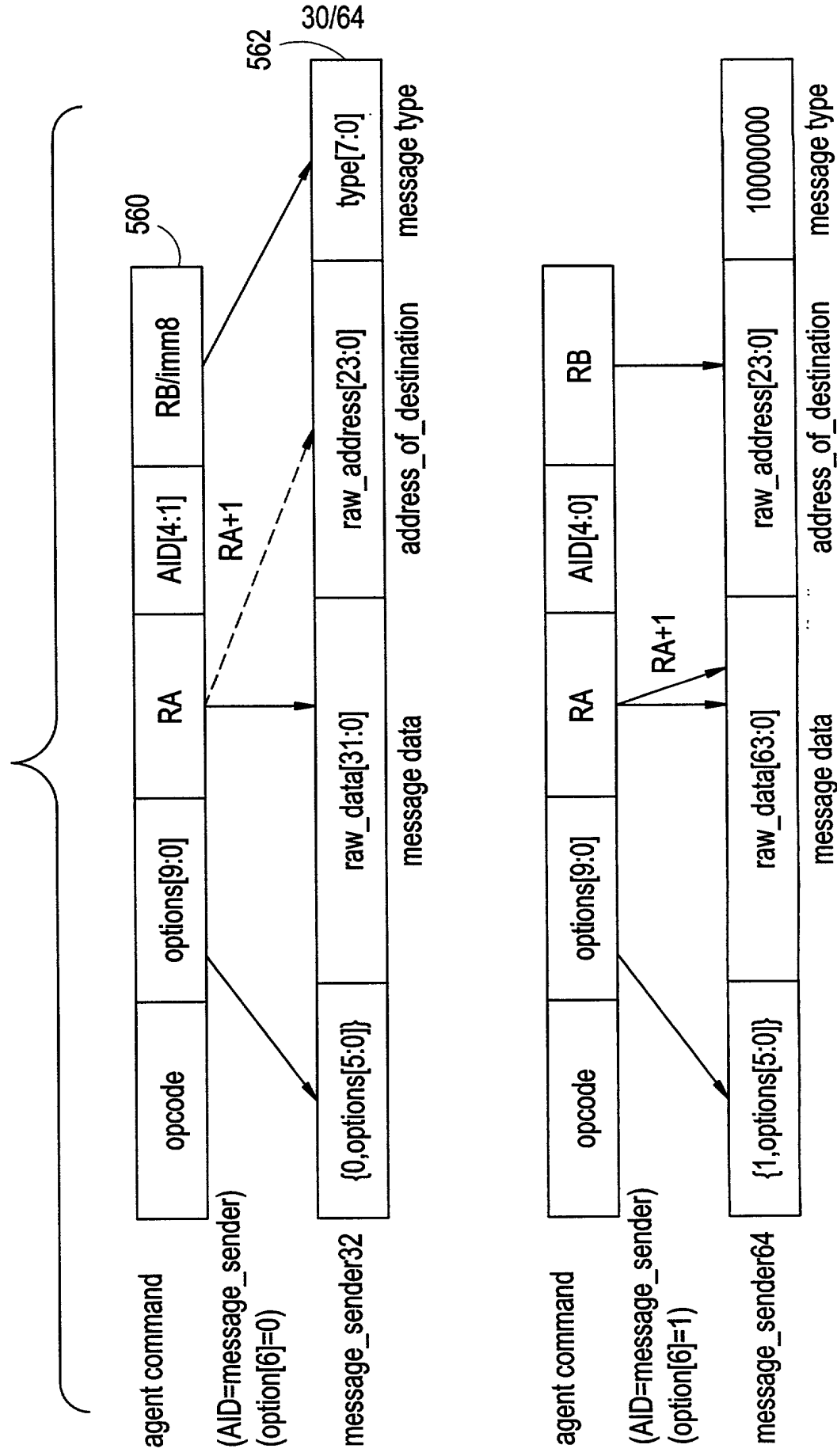


FIG. 53

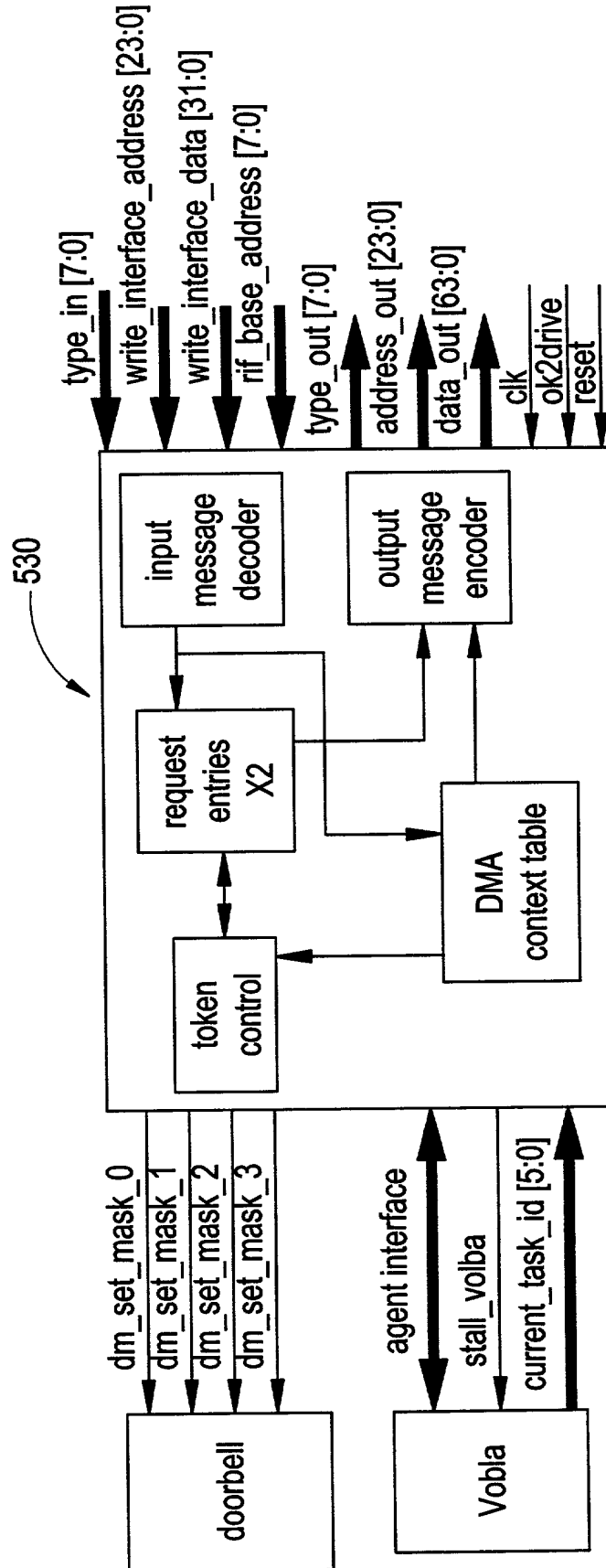


FIG. 54

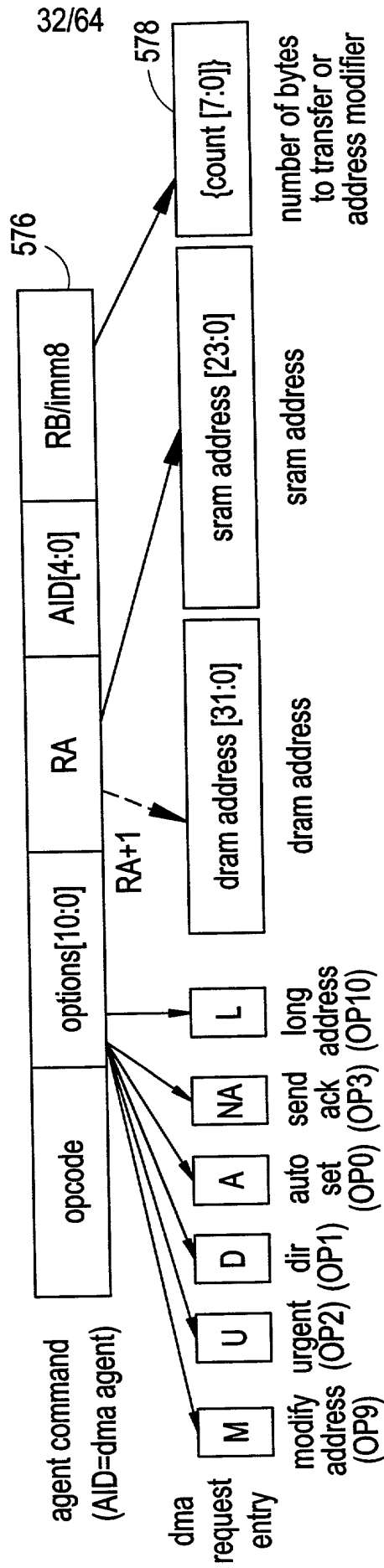
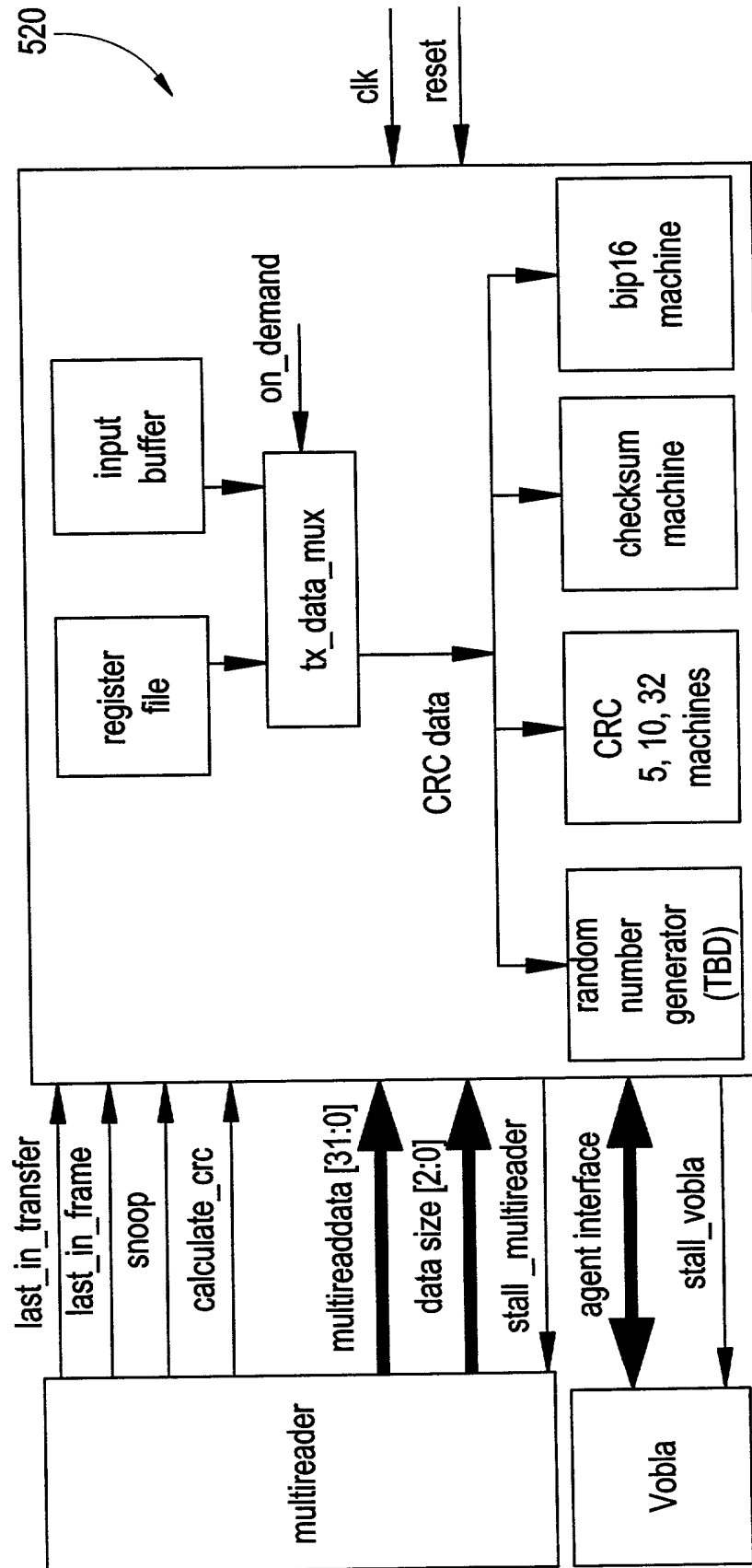


FIG. 55



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FIG. 56

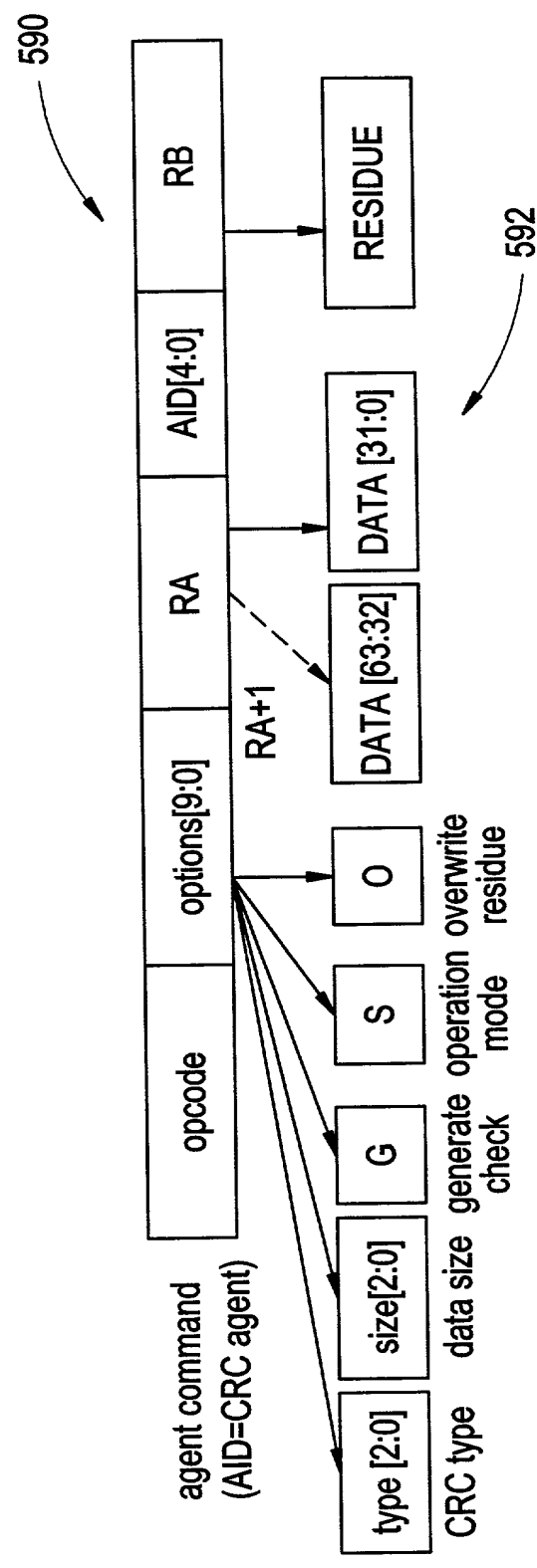


FIG. 57

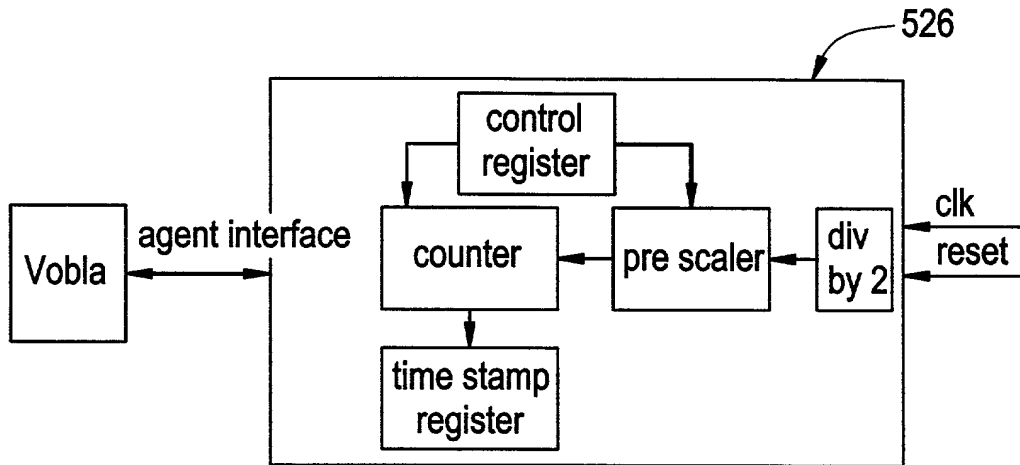


FIG. 58

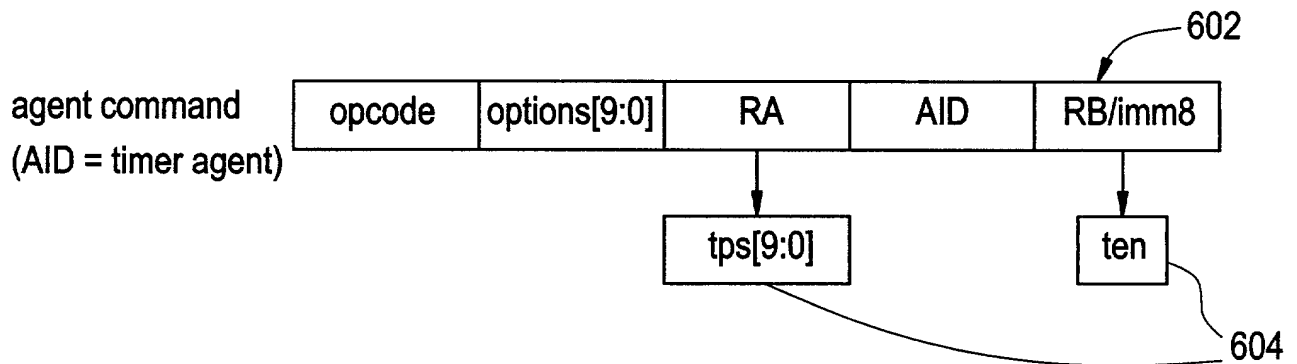


FIG. 59

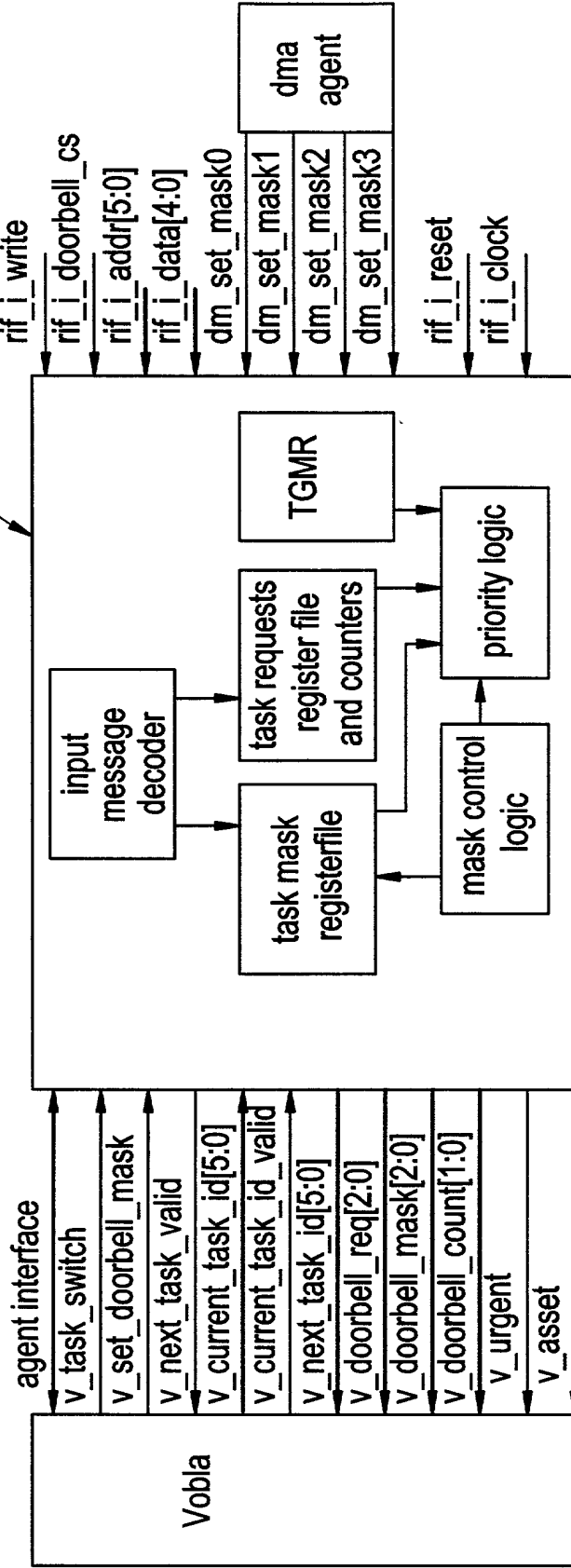


FIG. 60

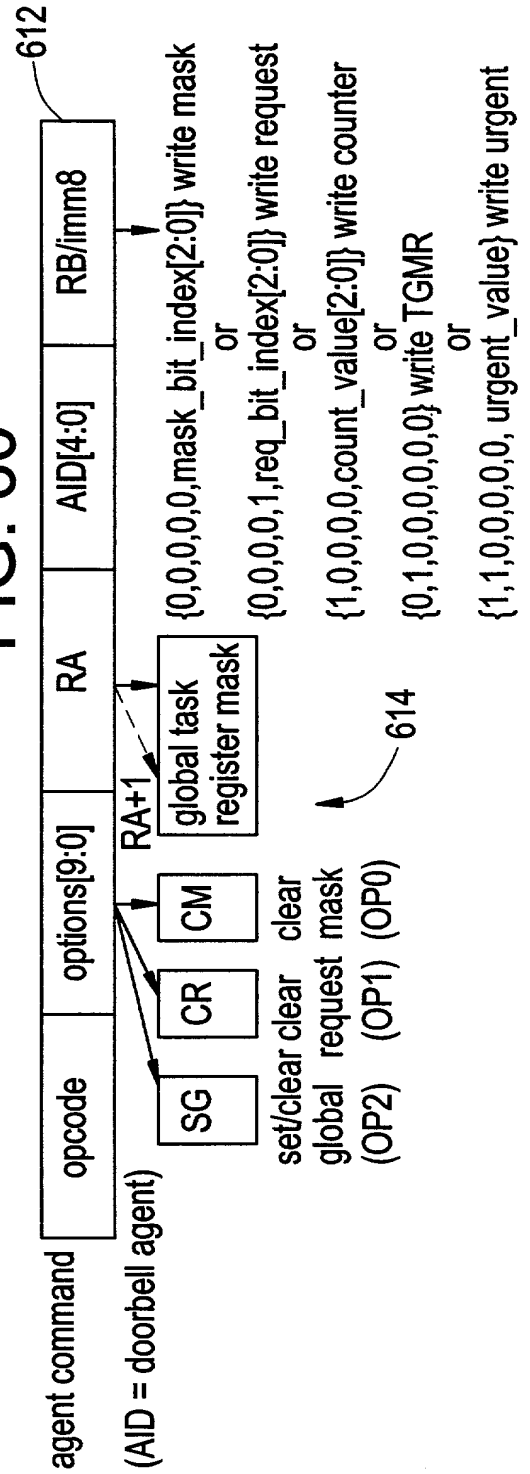
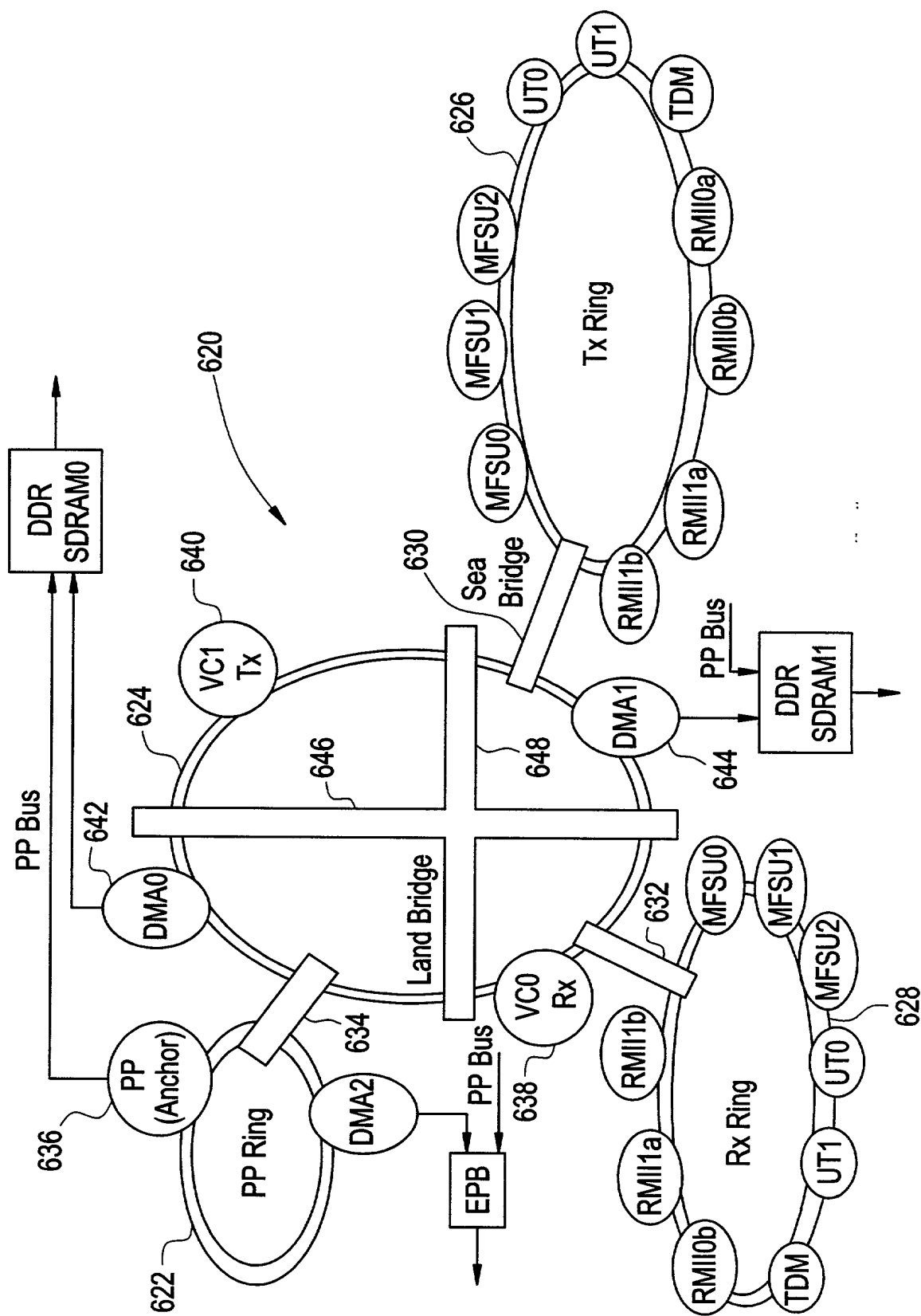


FIG. 61



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FIG. 62

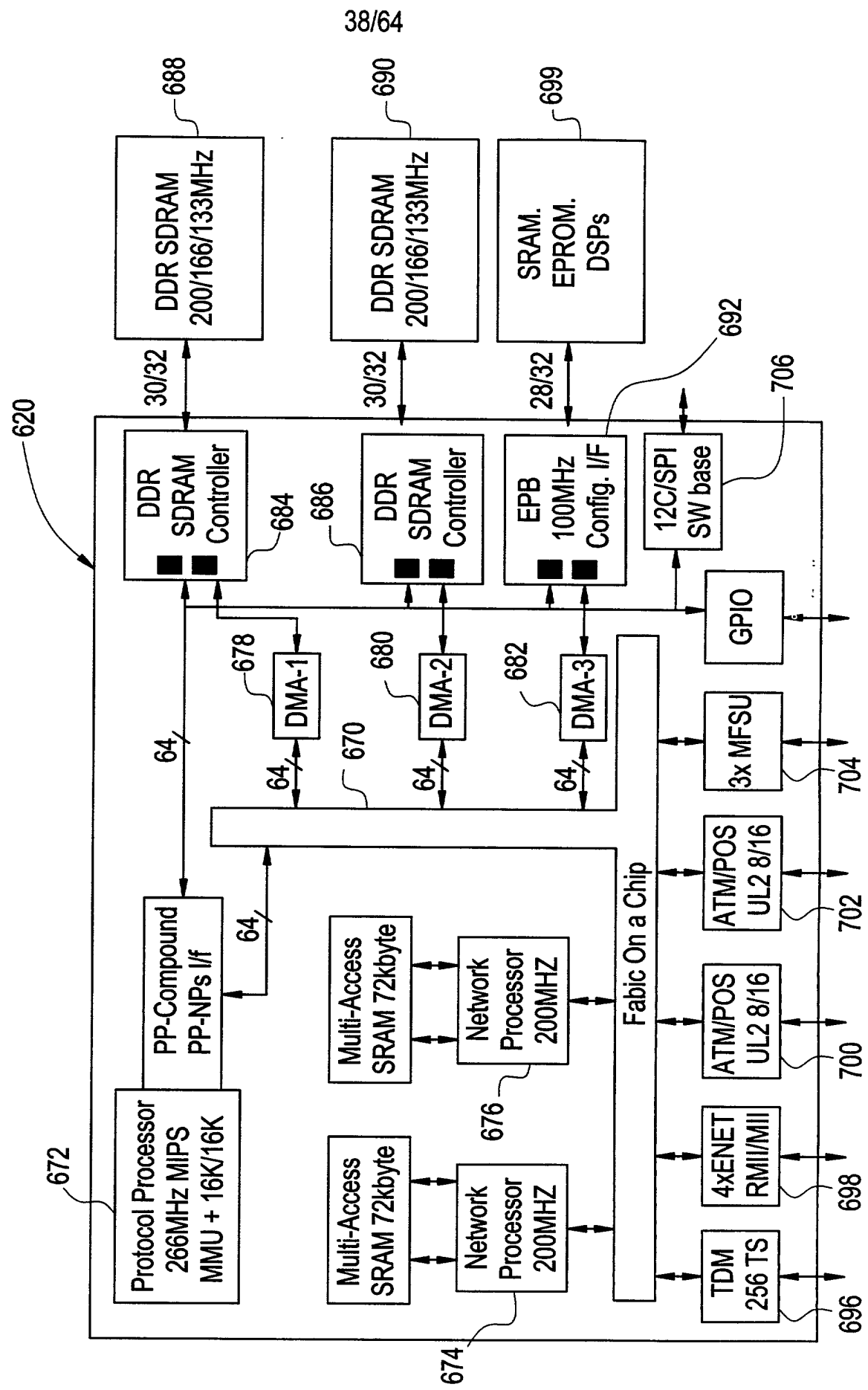


FIG. 63

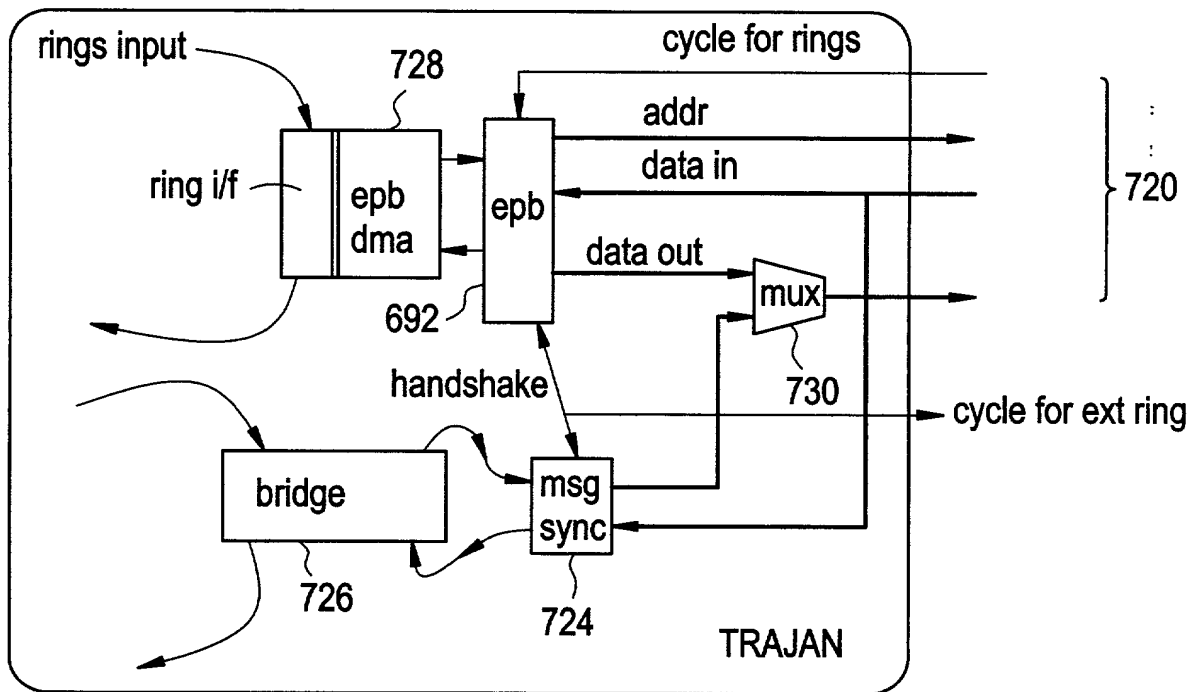


FIG. 64

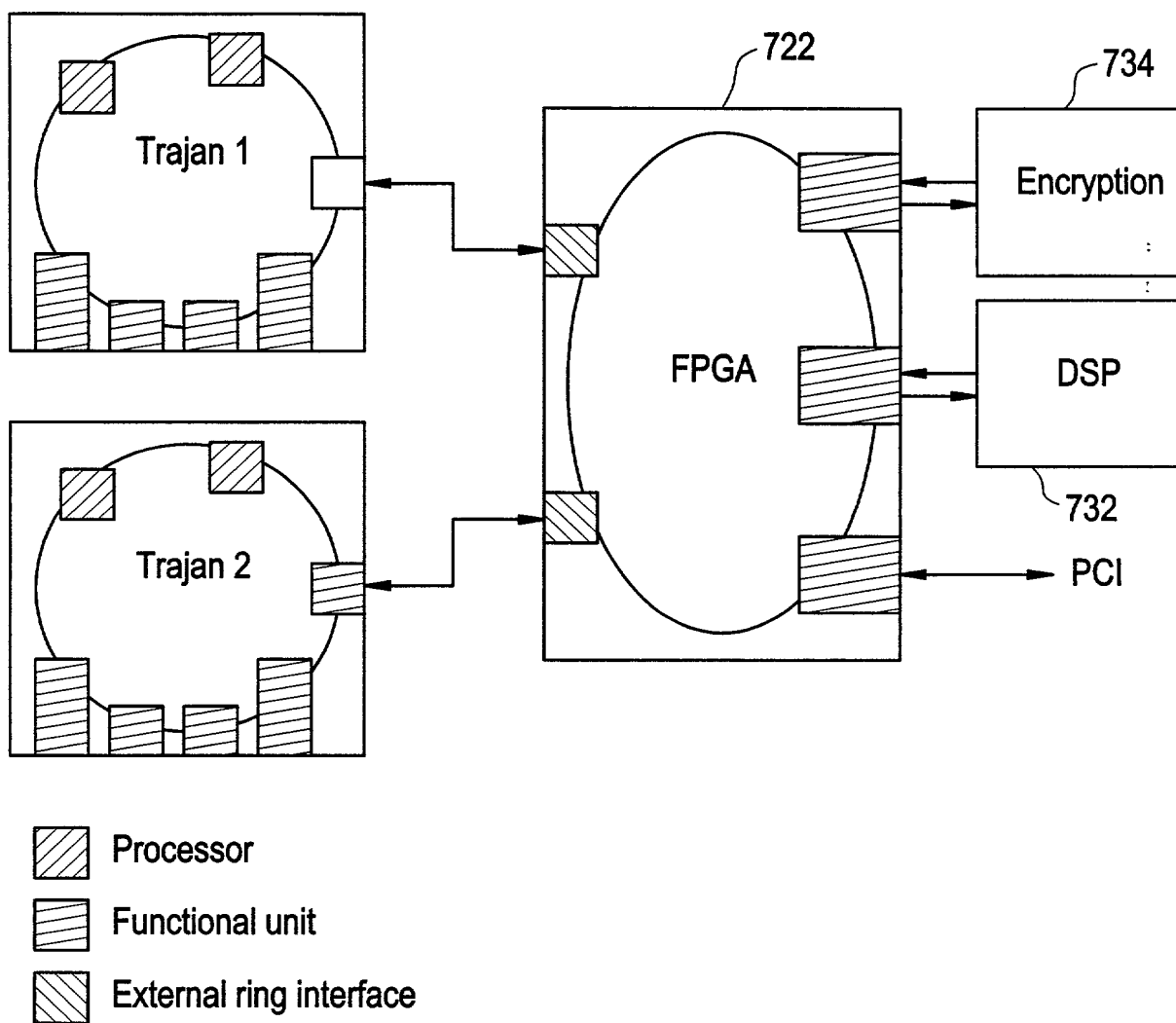


FIG. 65

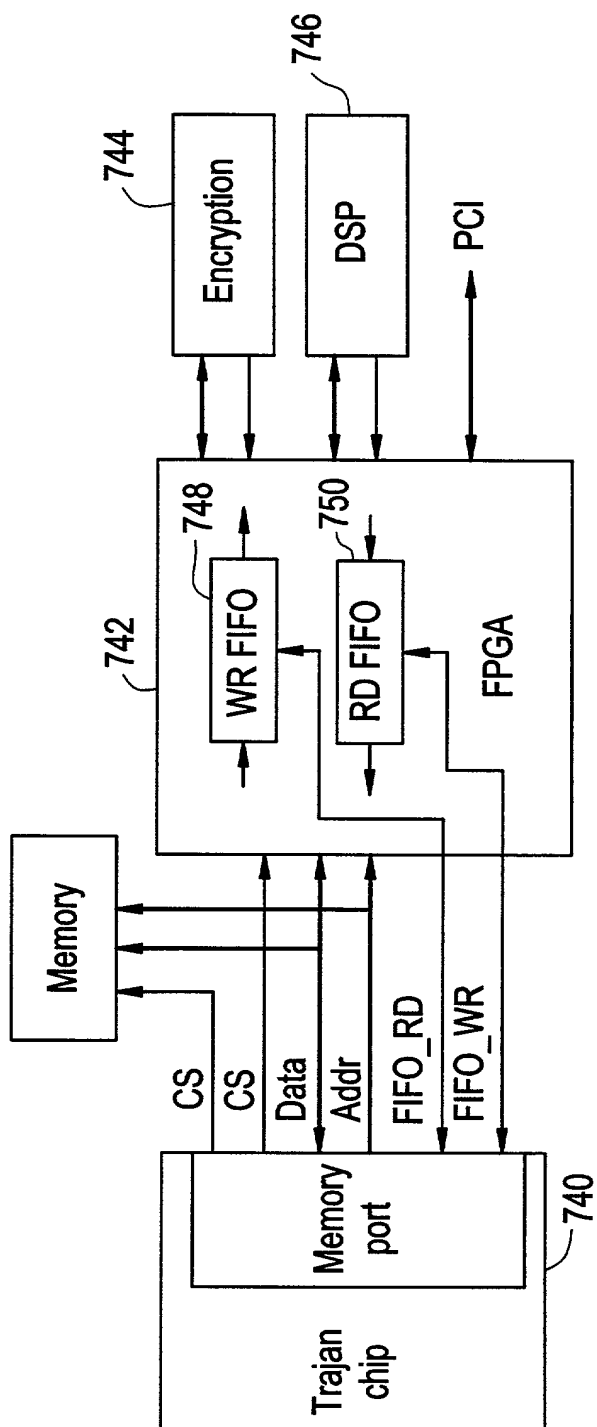


FIG. 66

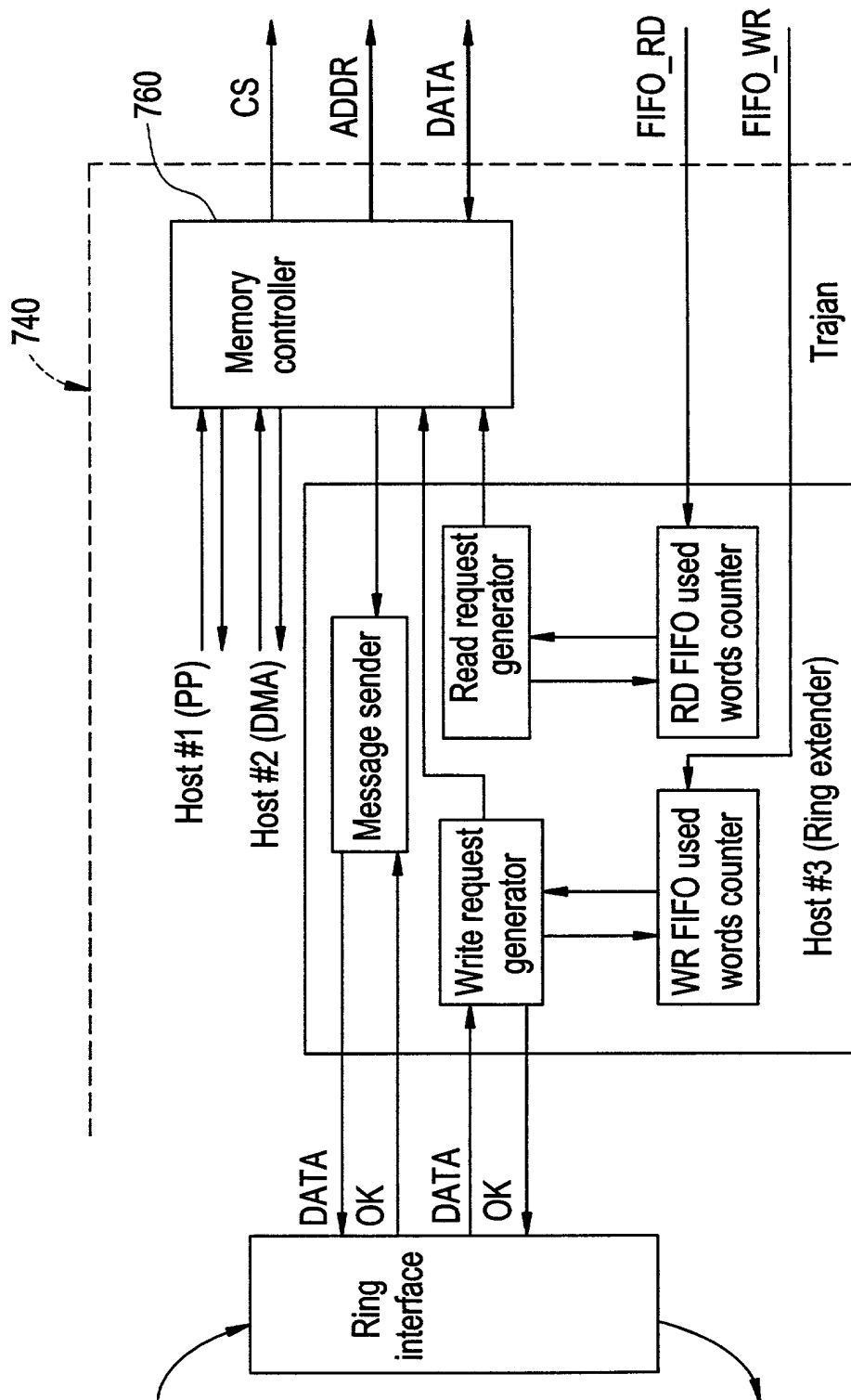


FIG. 67

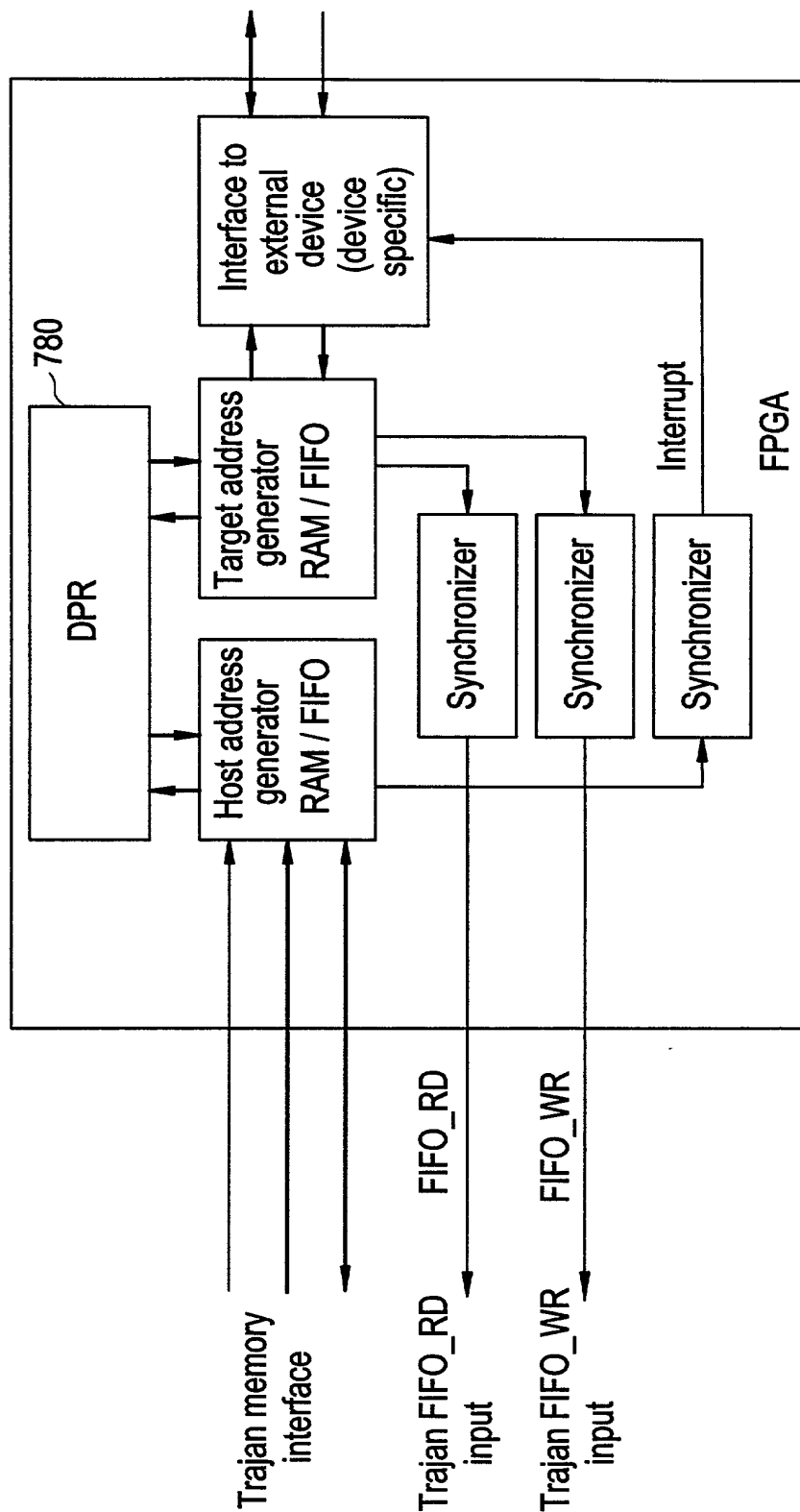


FIG. 68

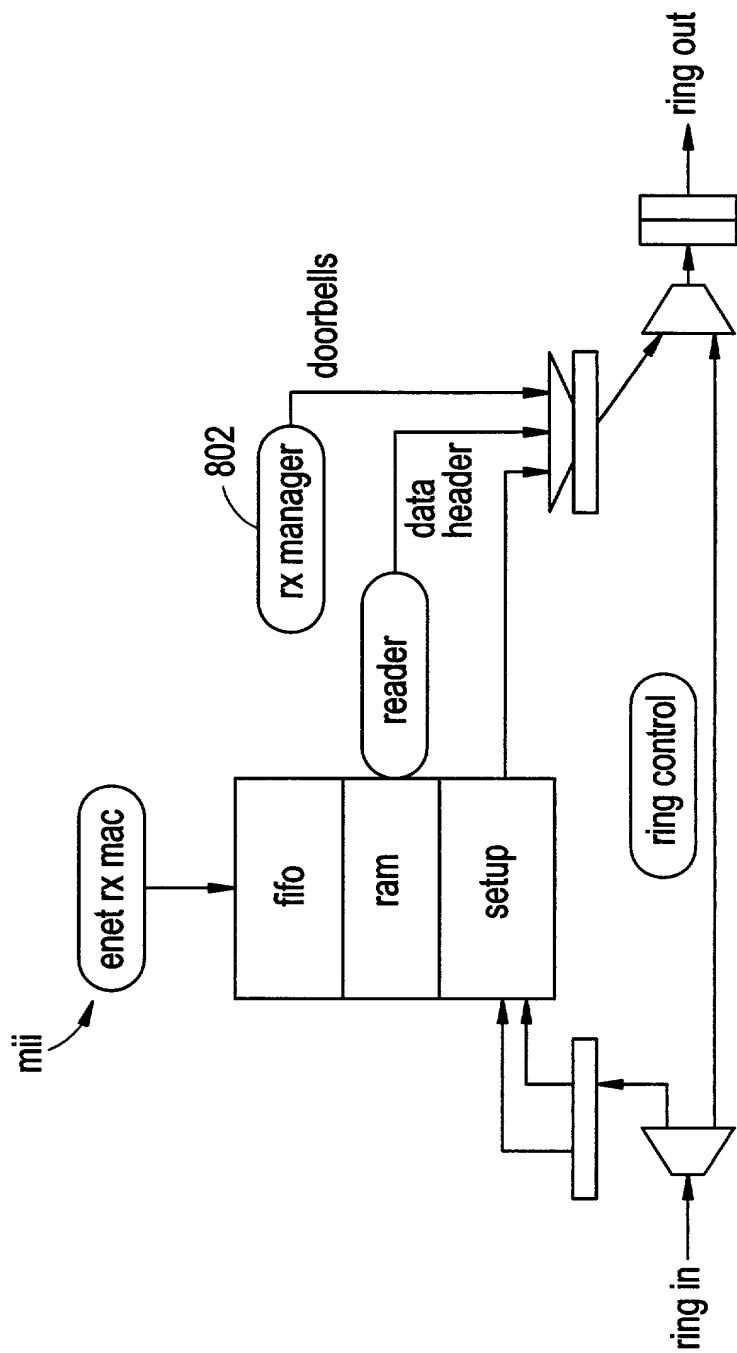


FIG. 69

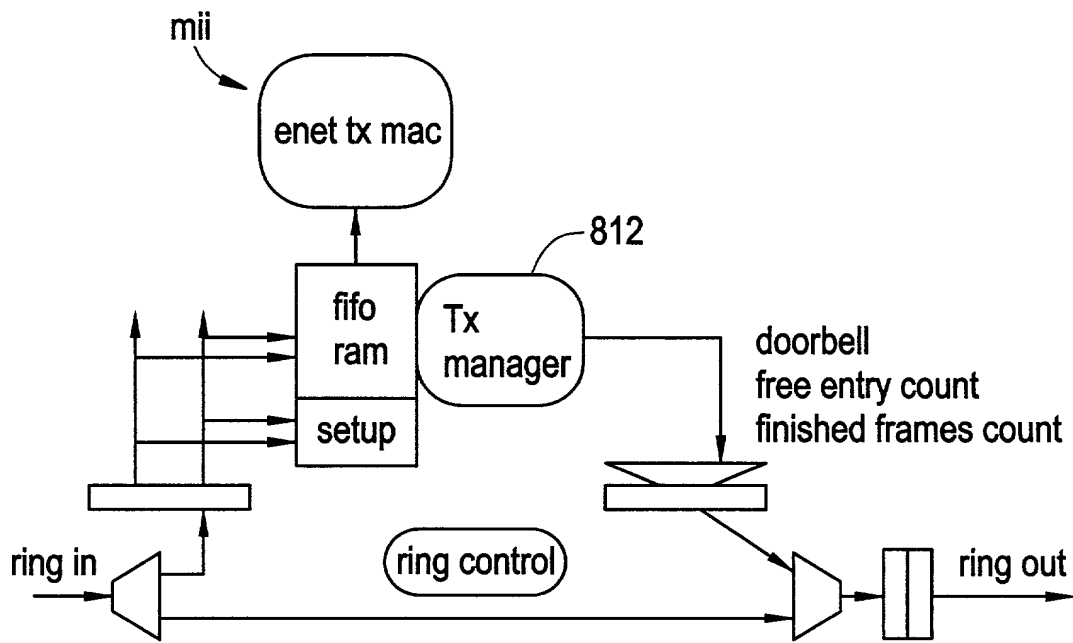
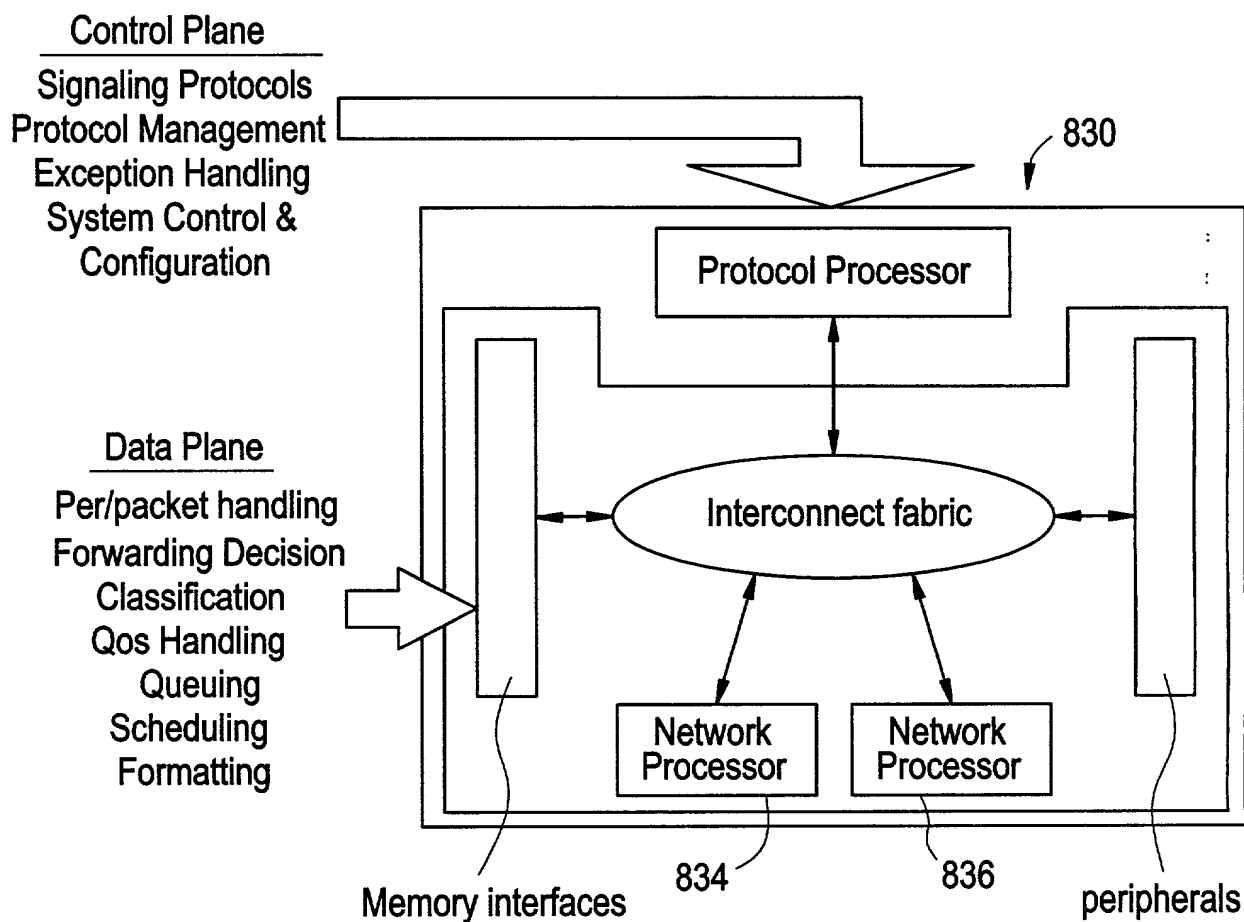


FIG. 70

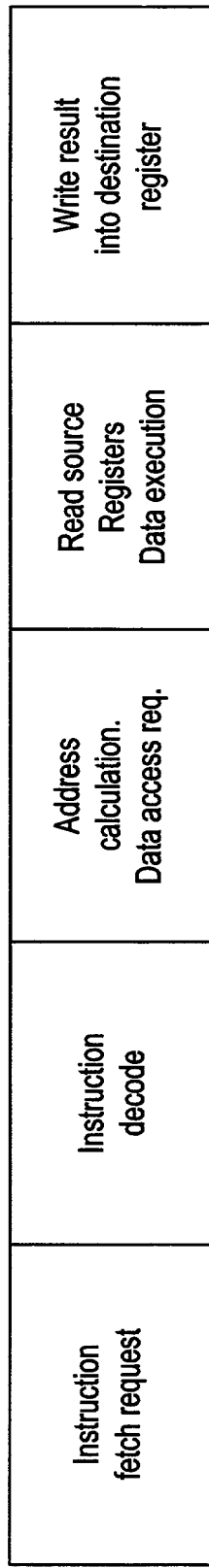
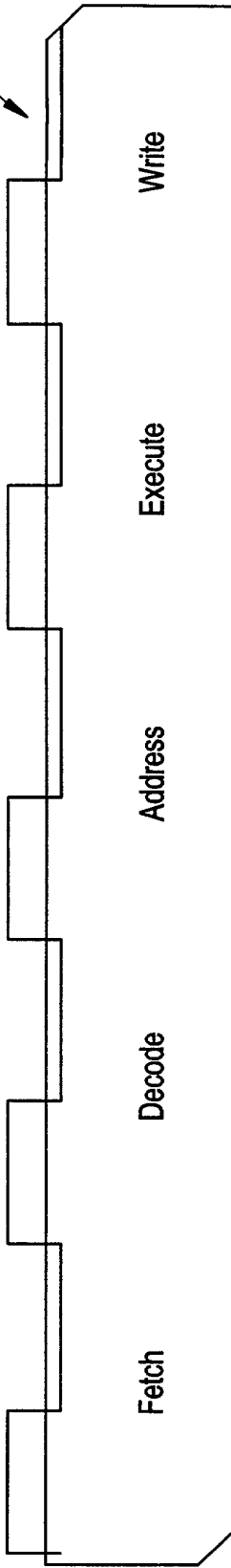


The diagram illustrates a complex network architecture with multiple layers and protocols. At the top, three main sections are shown: 'MGCP (SM)' and 'MEGACO (SM)' leading to 'UDP/TCP (SM)'; 'OSPF (SM)', 'BGP-4 (SM)', and 'RIP (SM)' leading to 'IP (SM)'; and 'MPLS (SM)' and 'RSVP-TE (SM)' leading to 'IP/ATM (SM)'. Below these, a central 'UNI' block is connected to 'Signaling (SM)' and 'ATM (SM)'. The core of the diagram features a large 'AAL-2' block with sub-sections 'L366.1 (2*)', 'L366.2 (2*)', and 'L363L2 (2)'. This core is connected to various other blocks: 'FRF.8 (2*)' and 'FRF.5 (2*)' on the left; 'Circuit Emulation Services (CES) (2*)' and 'Cell Switch (2*)' in the middle; 'RFC 1490 (2*)' and 'Frame Relay (2)' on the right; and 'MPLS (2.5)' and 'IP FWD (3)' at the bottom. Further down, there are blocks for 'AAL-0 (2)', 'AAL-1 (2)', 'AAL-2 (2)', and 'AAL-5 (2)'. These are connected to 'PPP ML-PPP (2)', 'HDLC (2)', and 'Transparent (2)'. The bottom-most layer includes 'Serial (1)', 'PCM (1)', 'ATM Low Layer Module (2)', and 'Utopia Interface (1)'. External connections include '802.1D Bridge (2*)', 'RFC 1483 (2*)', 'IPoA & PPPoA (2*)', and 'PPPoE (2*)' leading to an 'Ethernet (1)' block.

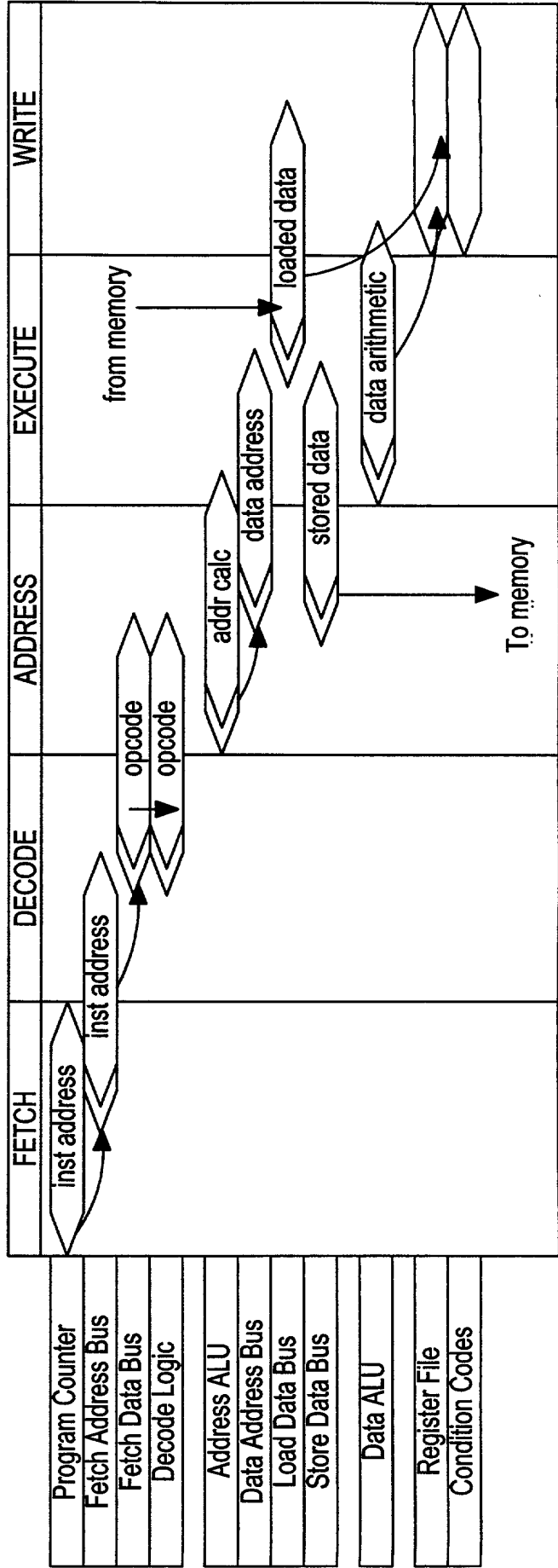
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FIG. 73

900



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◇ - Flip Flop
 ◇ - Logic

FIG. 74

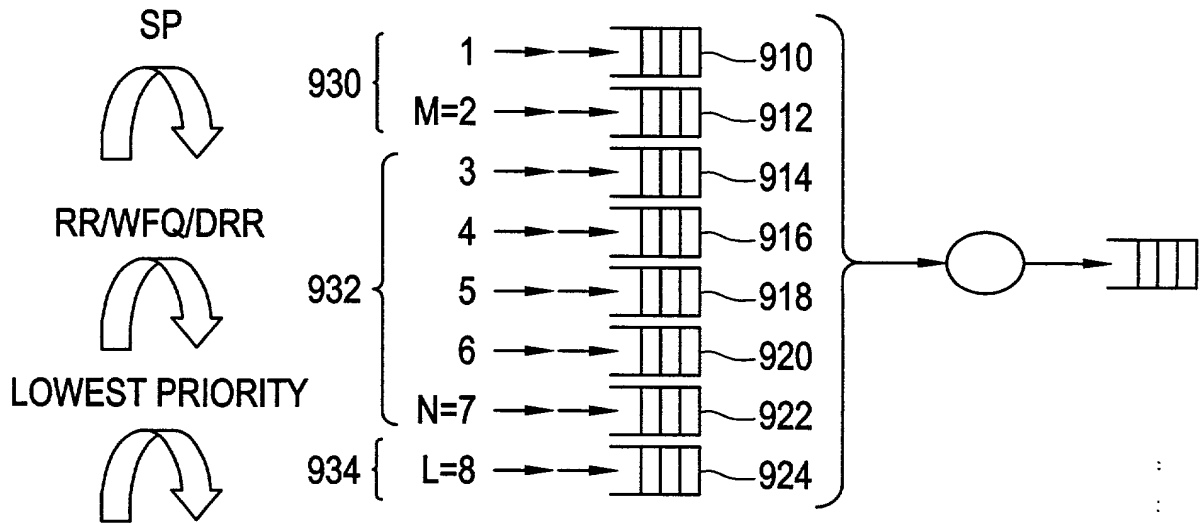


FIG. 75

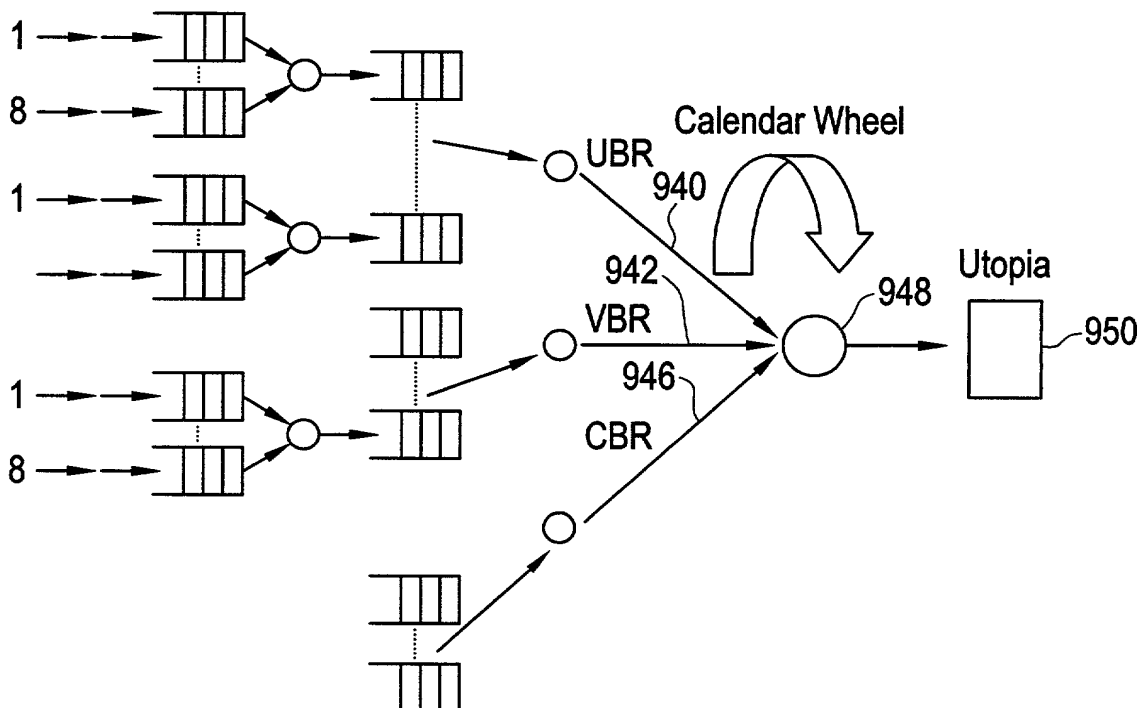
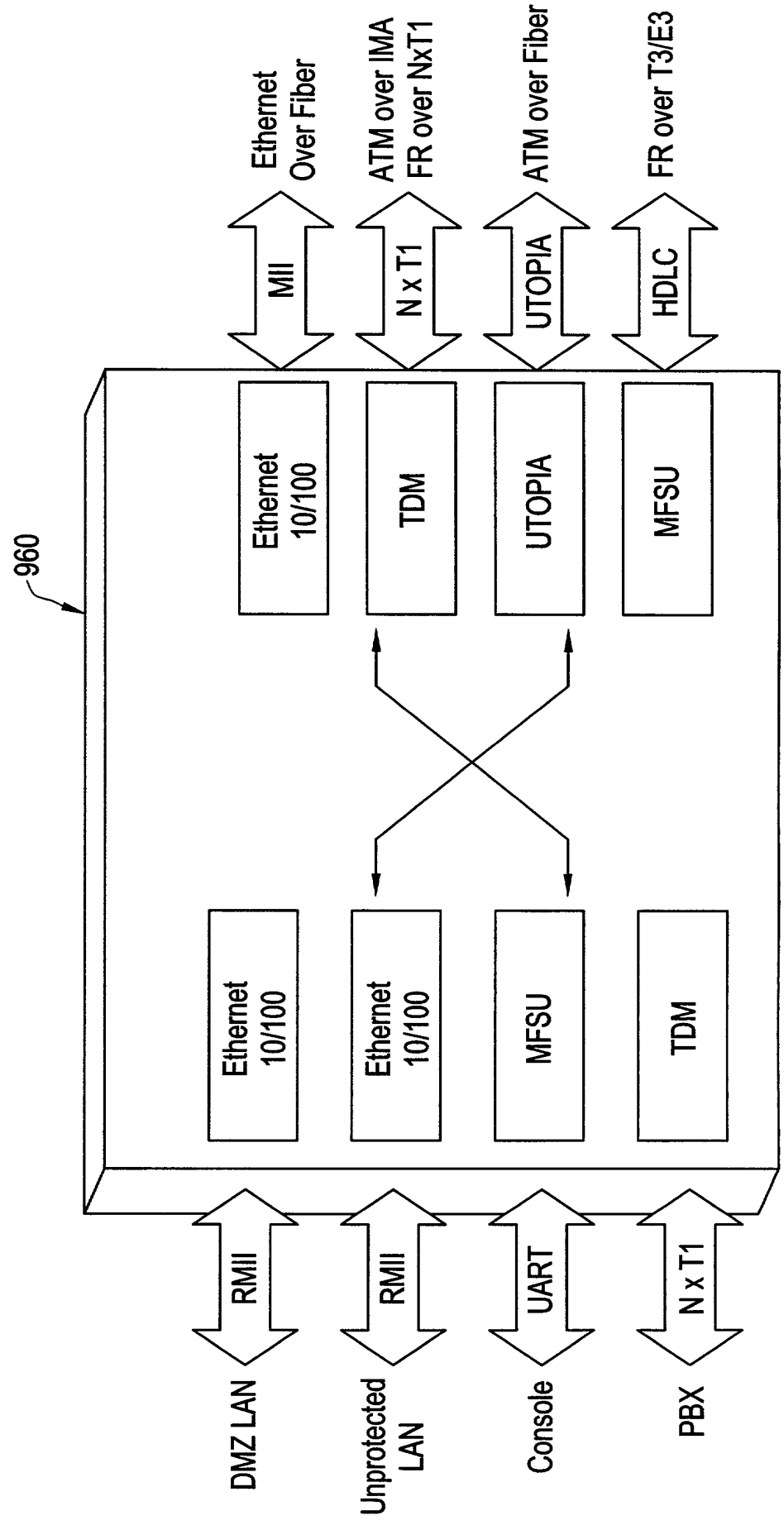


FIG. 76



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FIG. 77

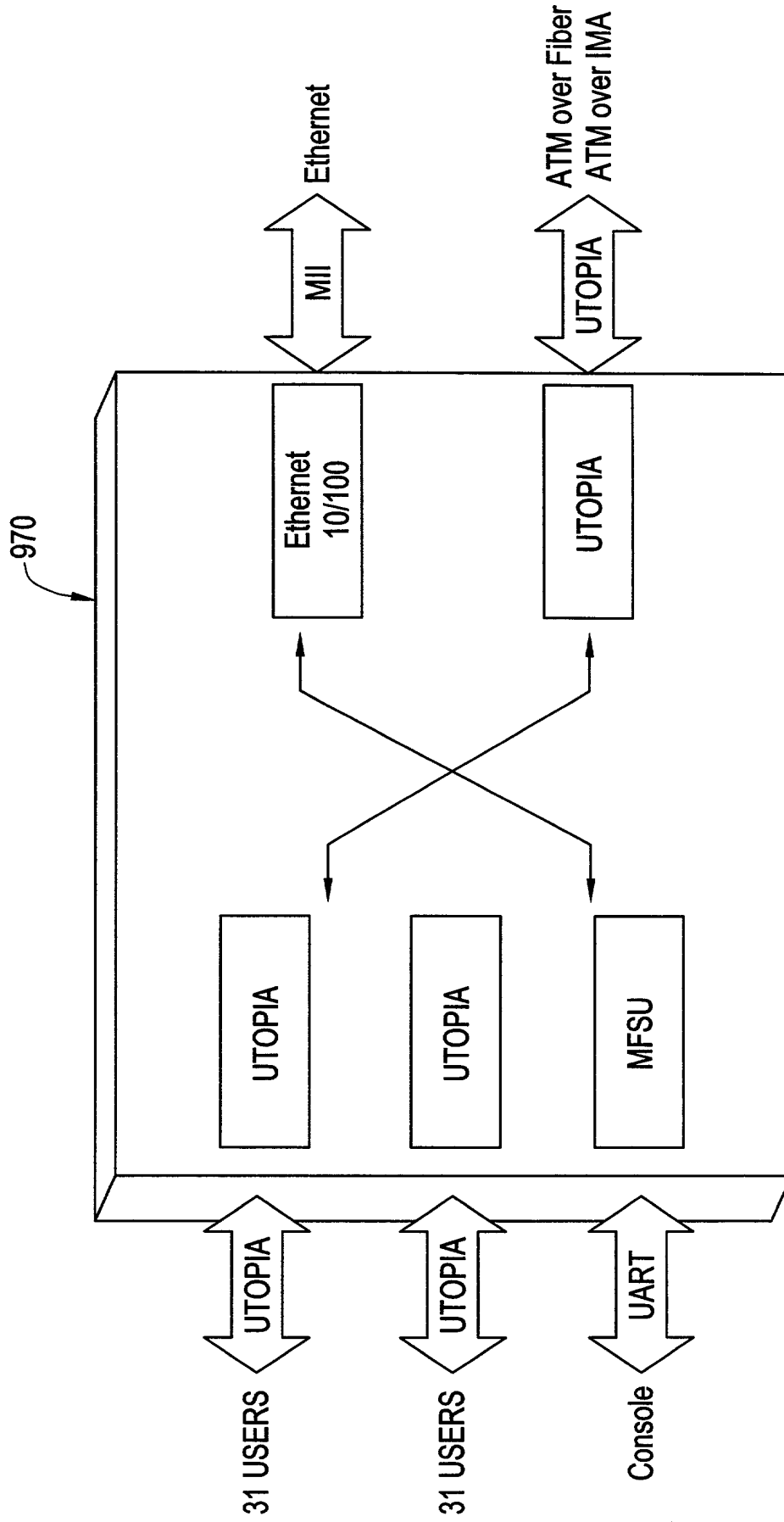


FIG. 78

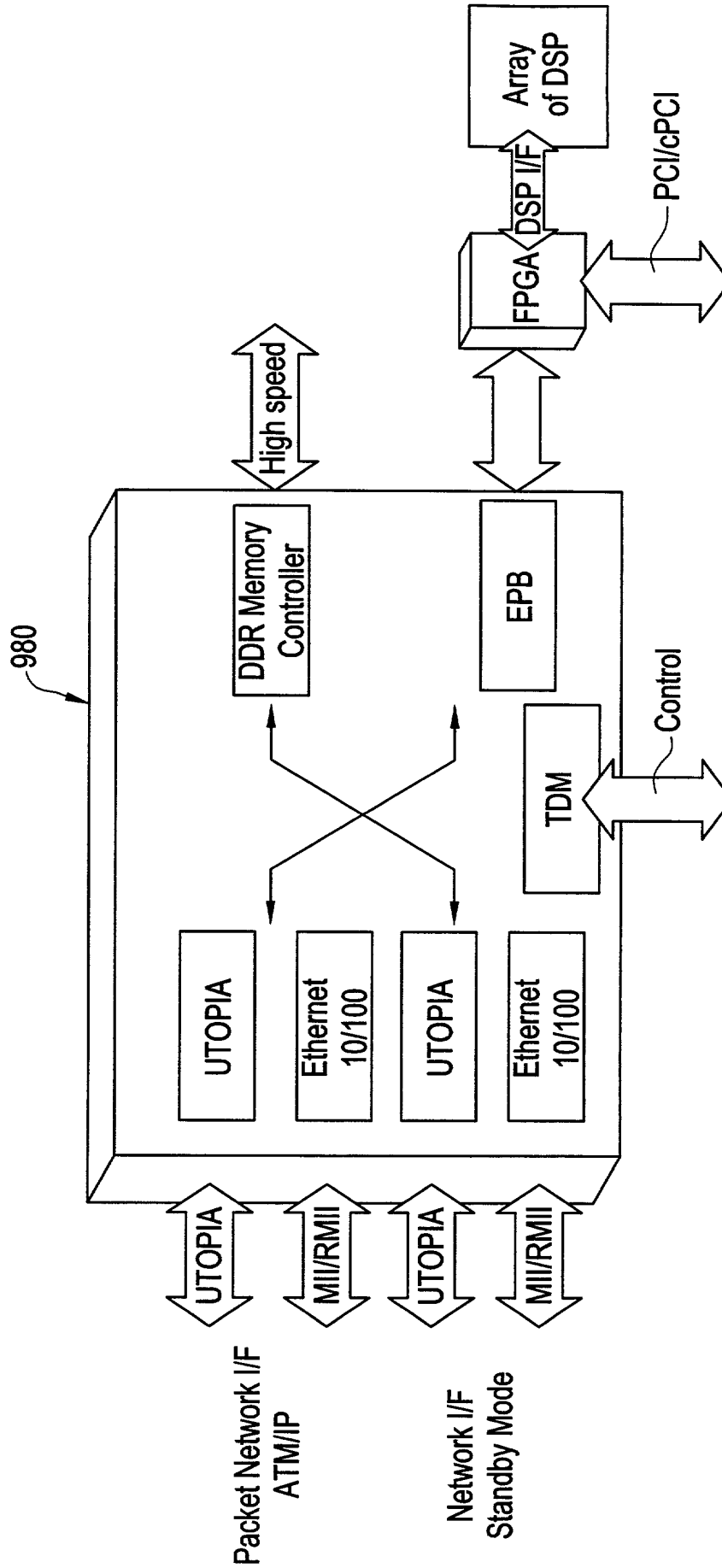


FIG. 79

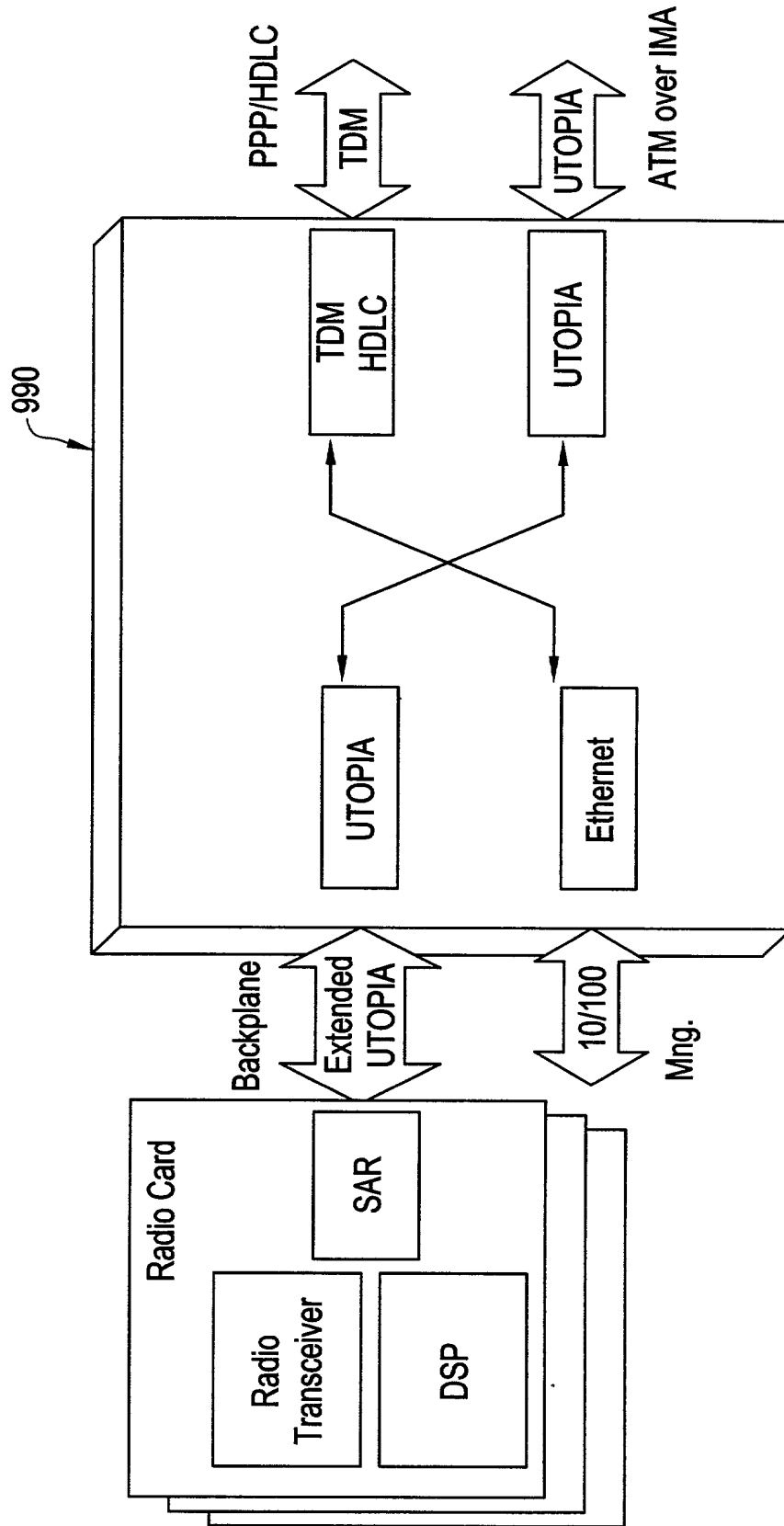


FIG. 80

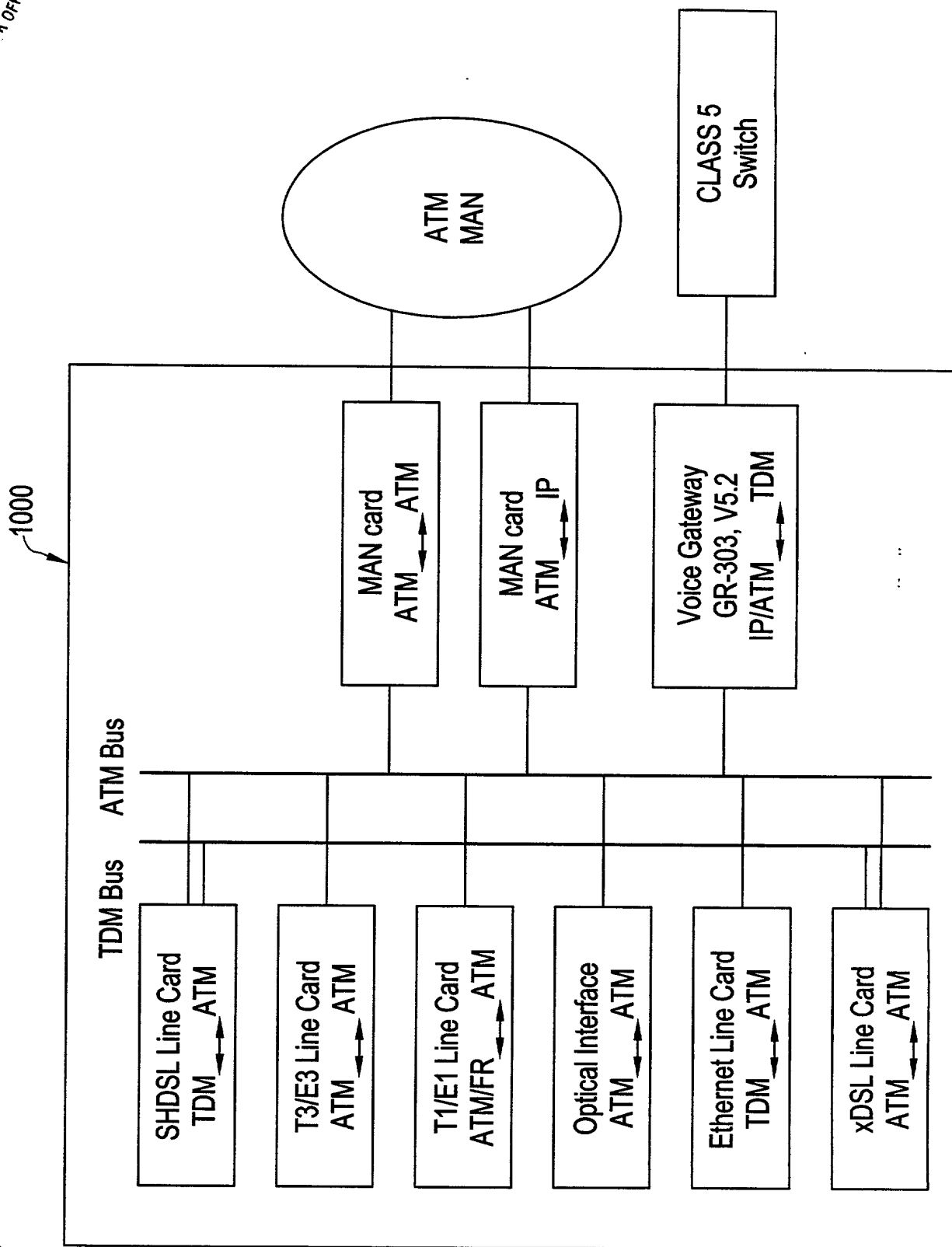


FIG. 81

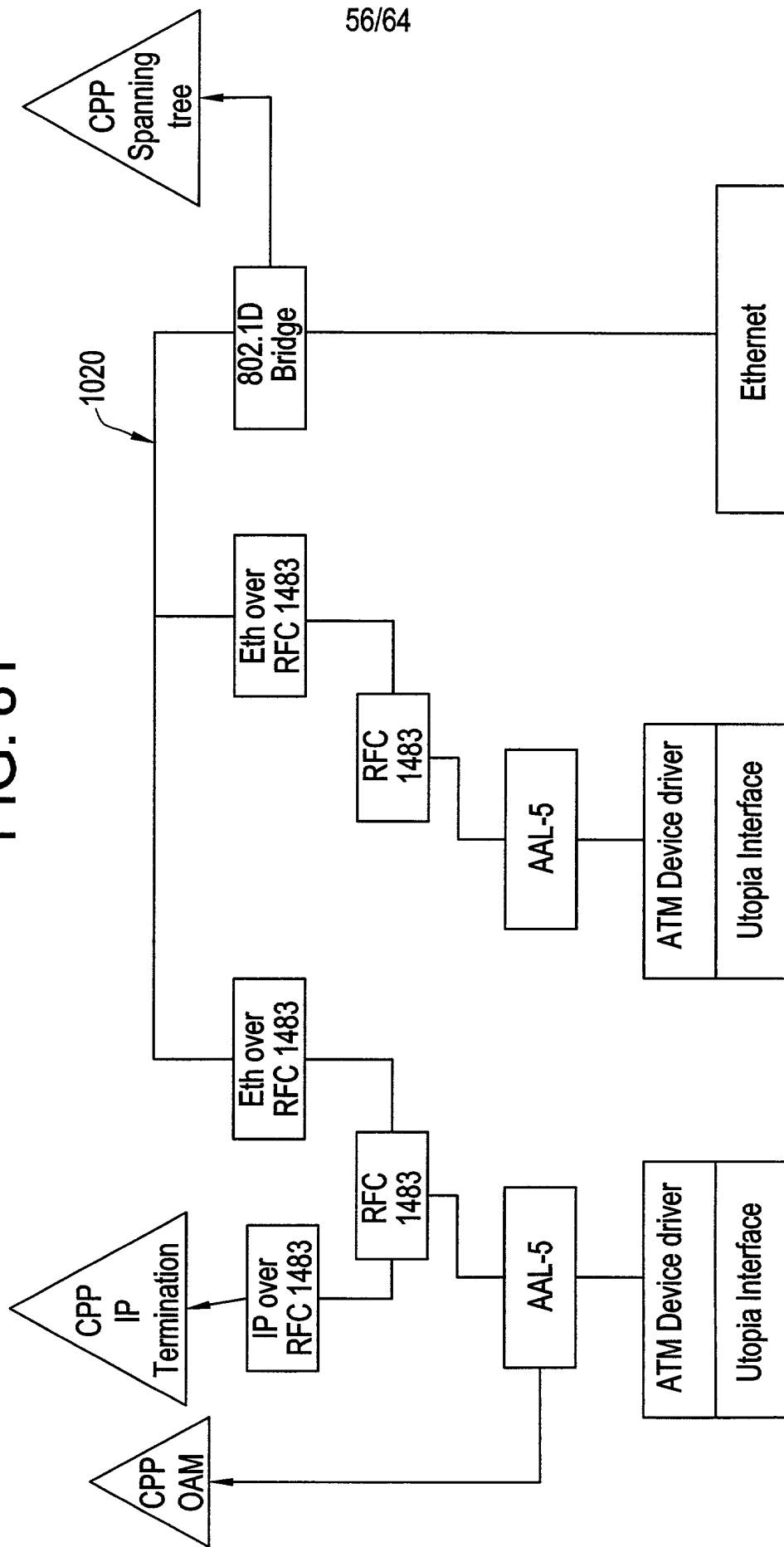


FIG. 82

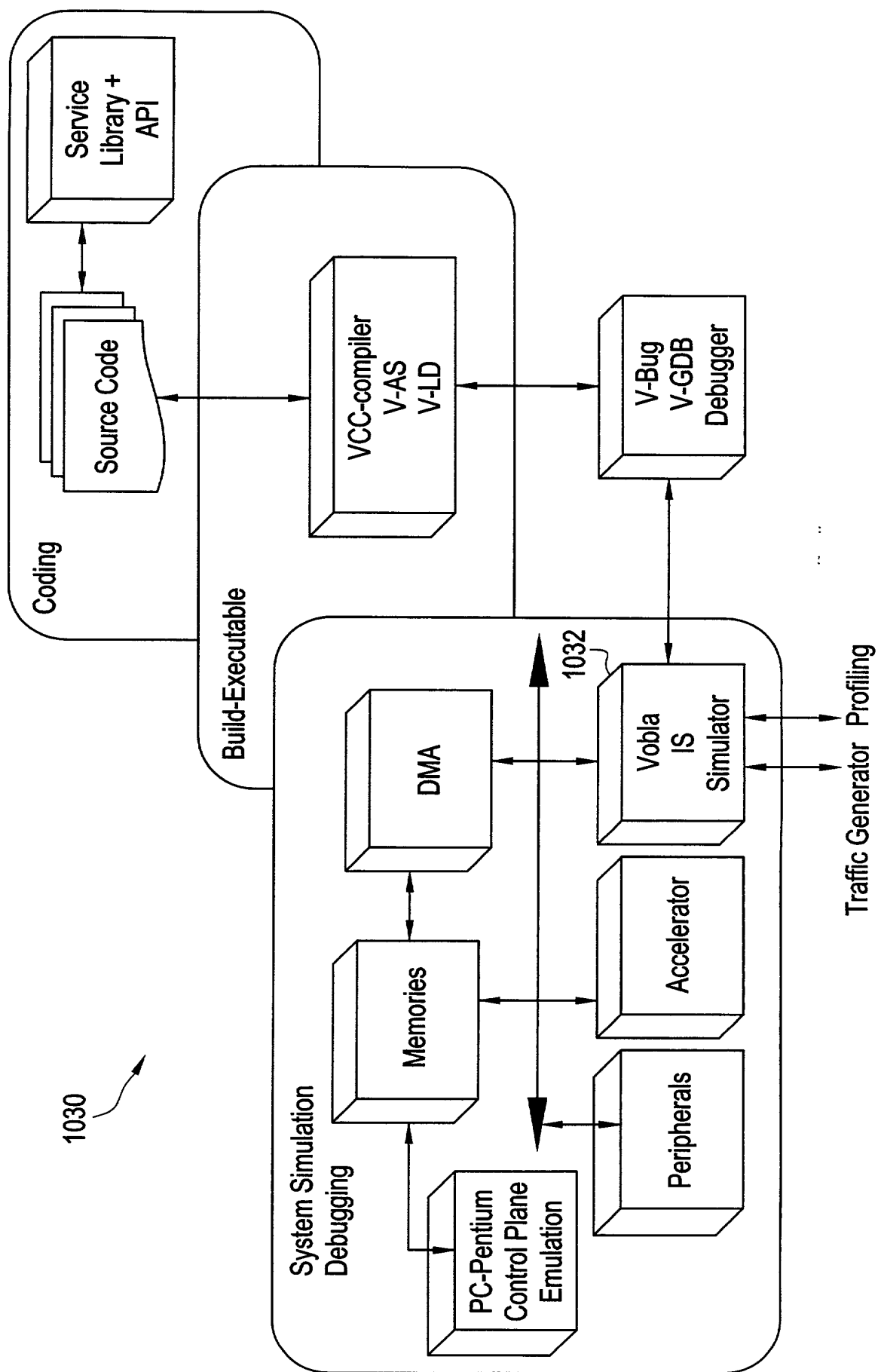
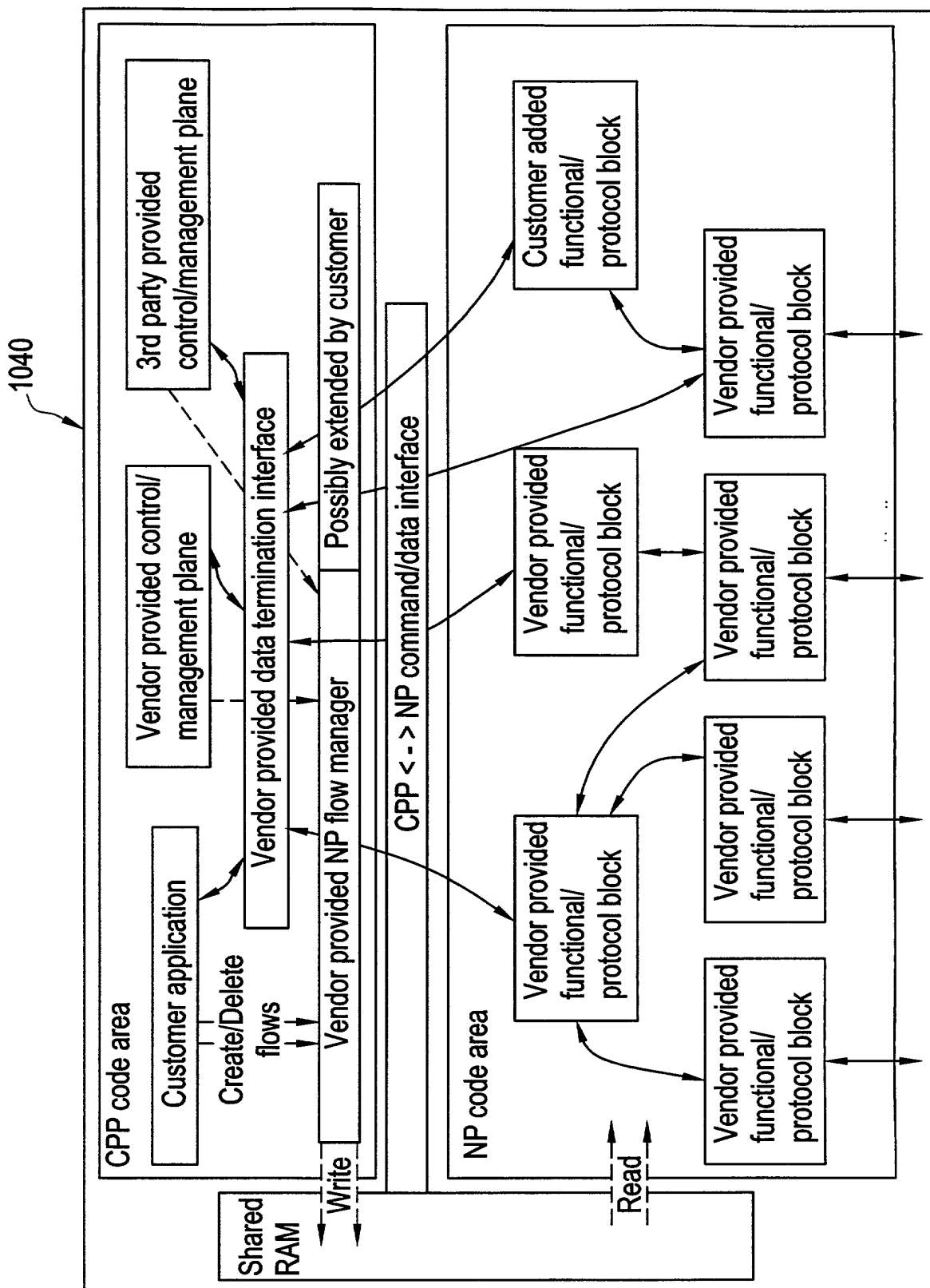


FIG. 83



1050

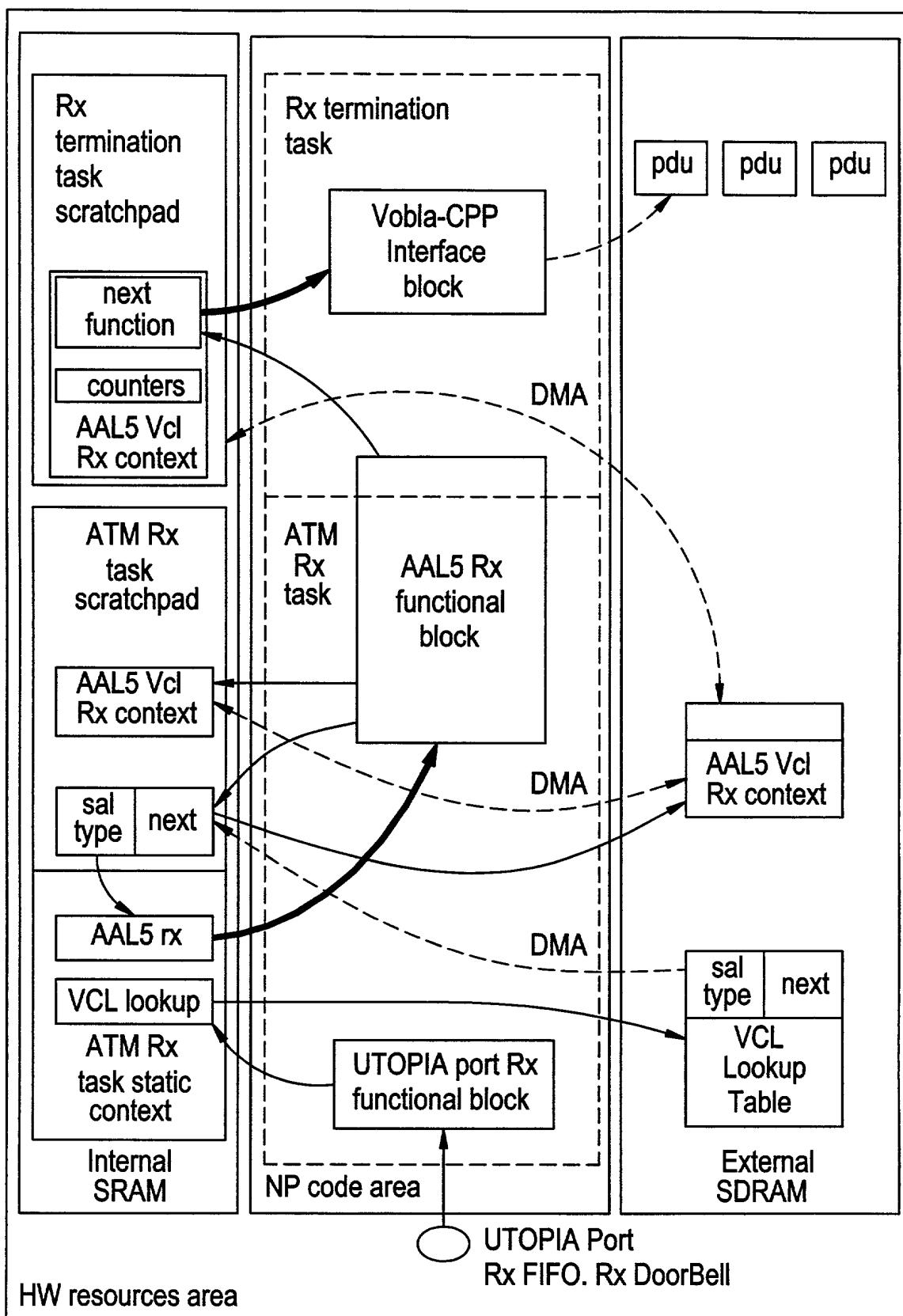


FIG. 85

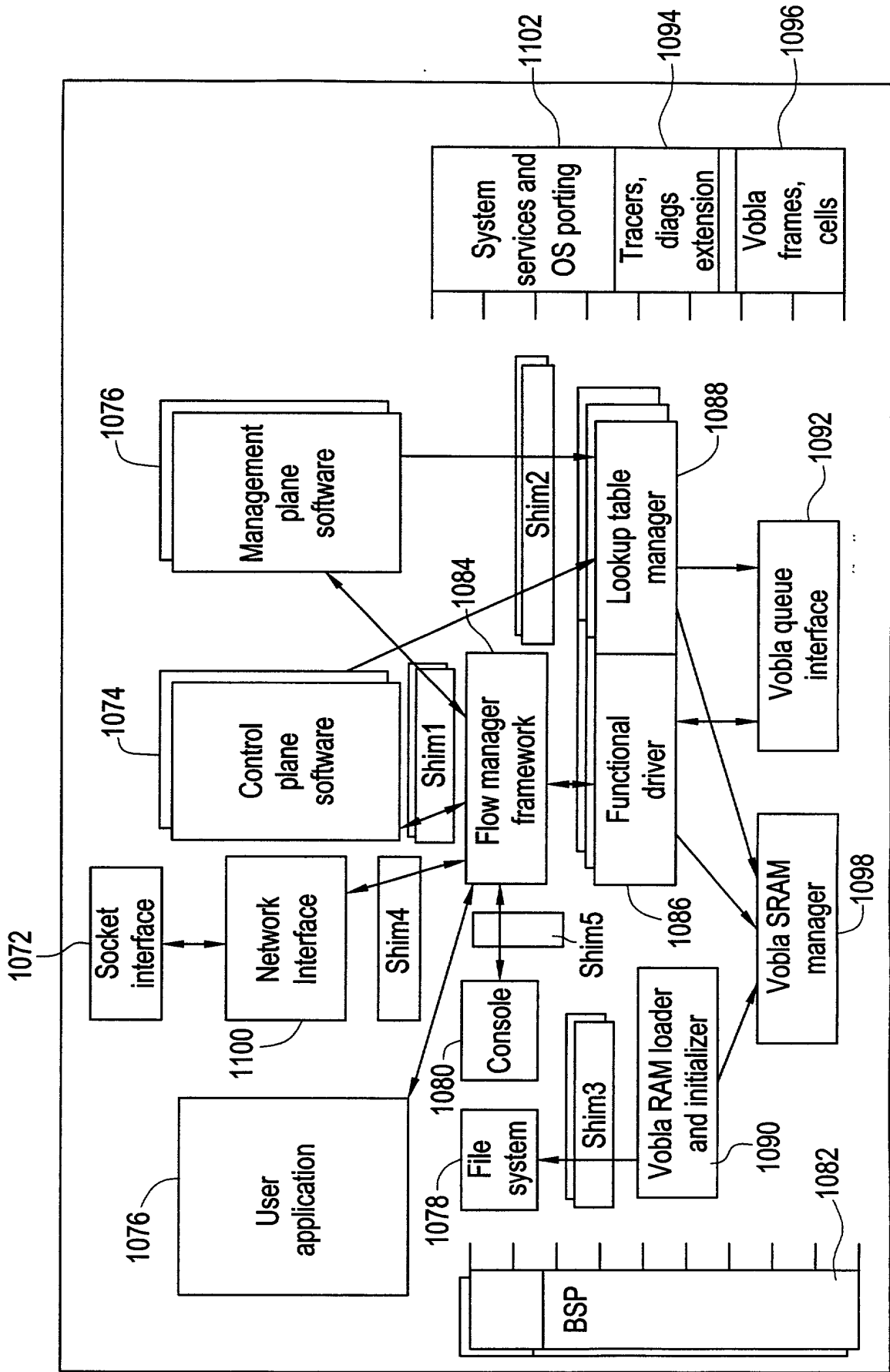


FIG. 86

1200

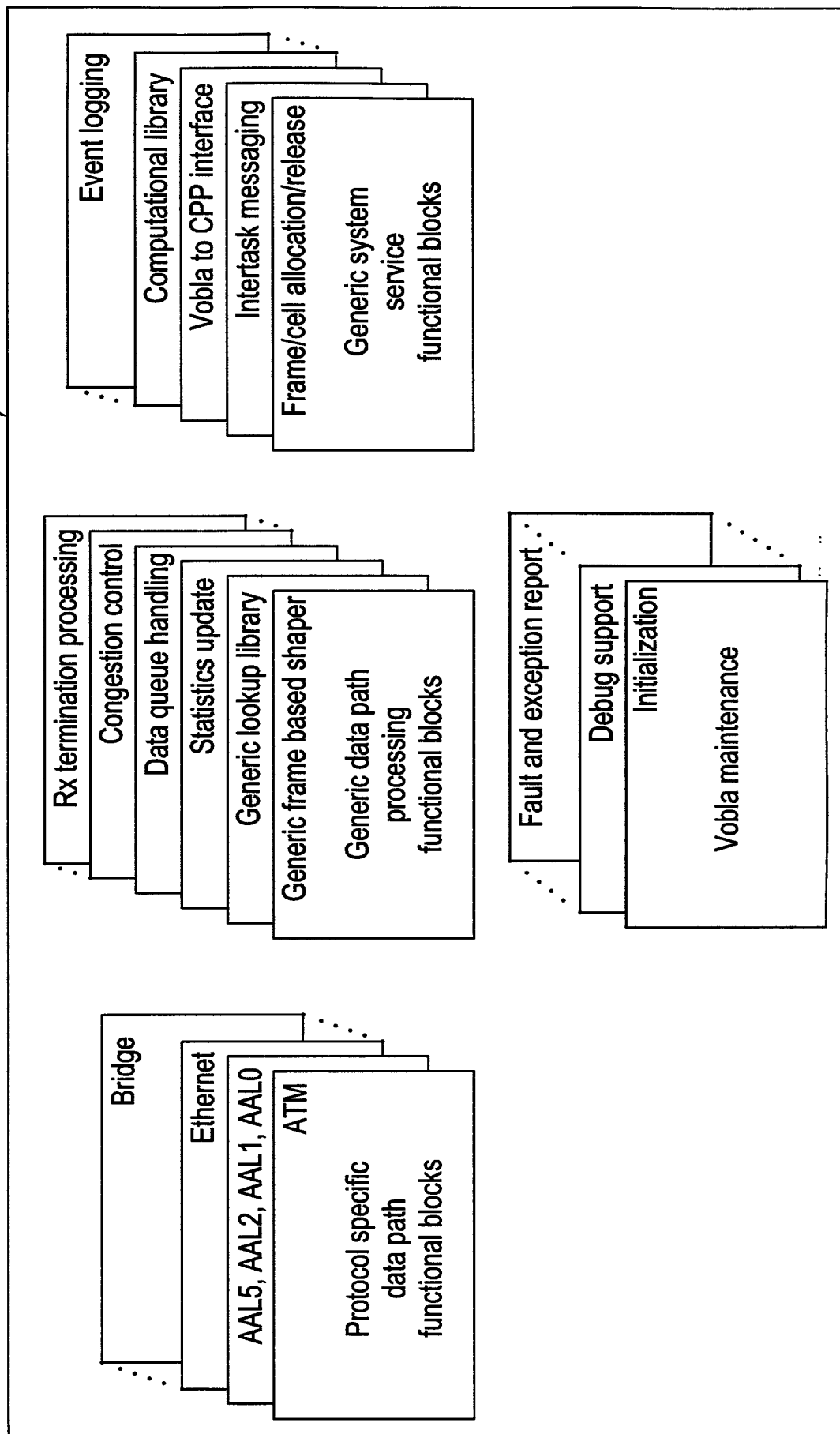


FIG. 87

PRIOR ART

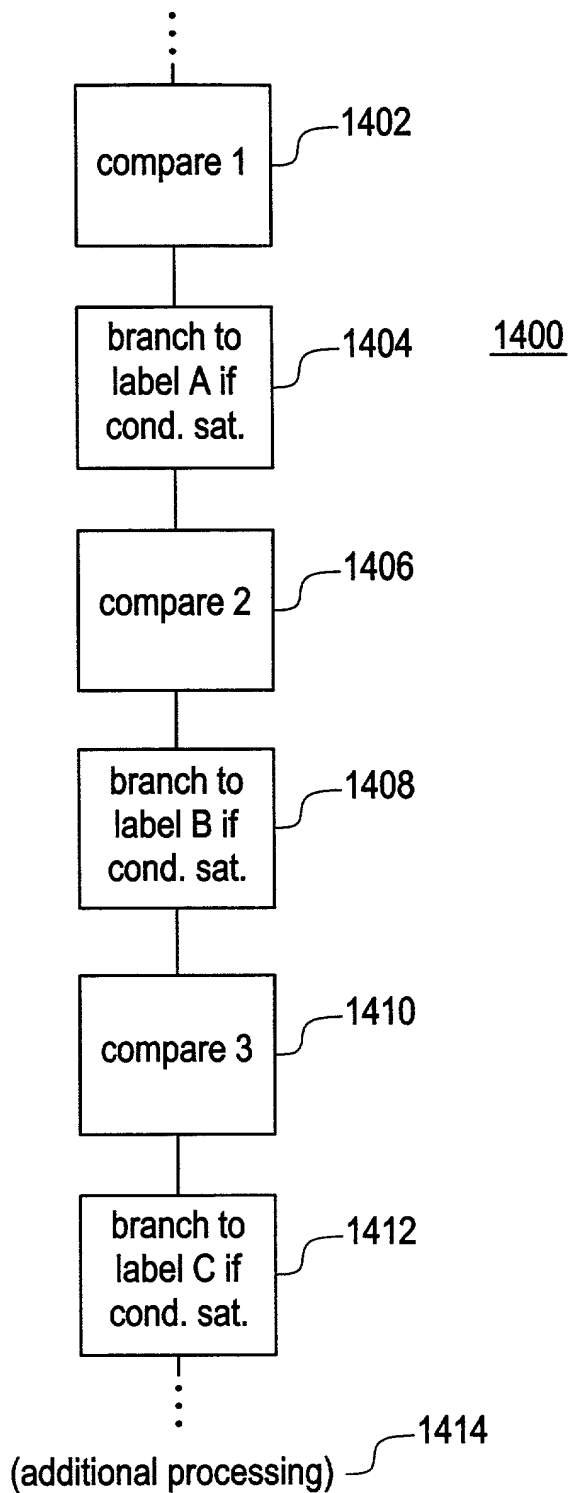


FIG. 88

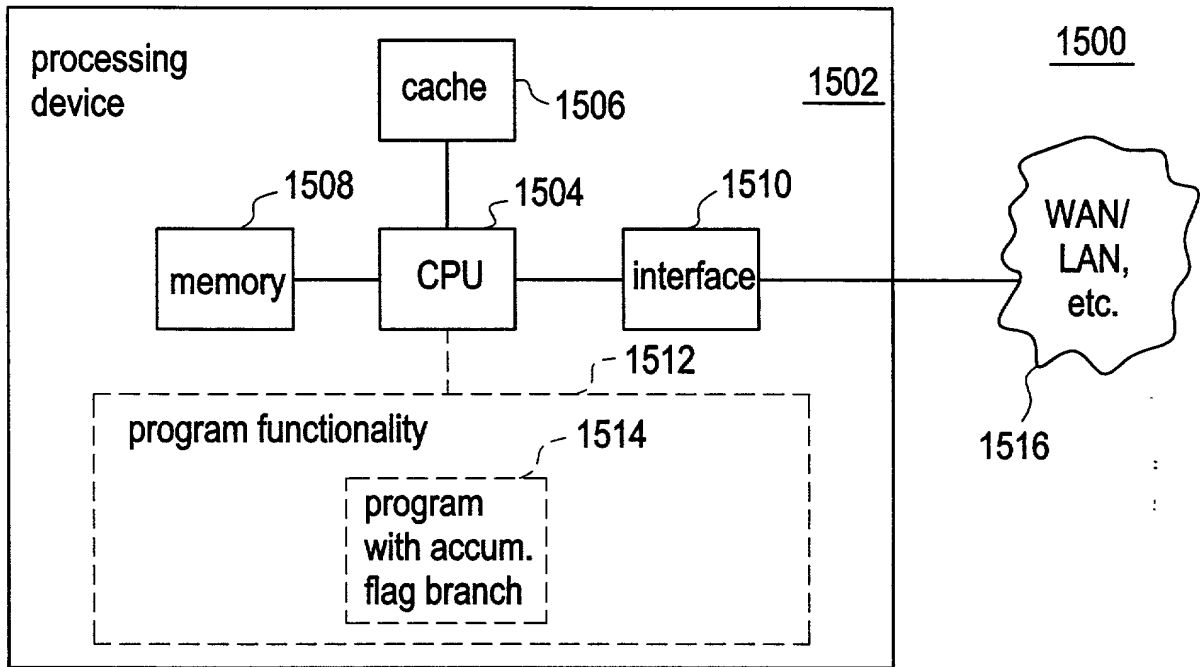


FIG. 89

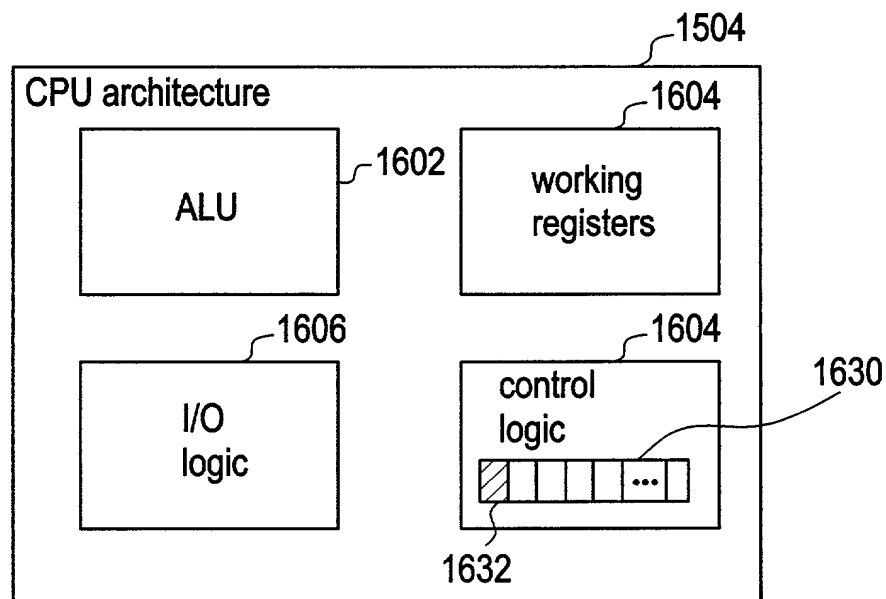


FIG. 90

